

IBM[®] Customer Engineering

Manual of Instruction

7600 Input/Output Control

7603 Input/Output Synchronize

F. IBM 7600 INPUT/OUTPUT CONTROL
IBM 7603 INPUT/OUTPUT SYNCHRONIZER

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FOREWORD

This manual is intended for use in training Customer Engineers in the operation of the 7600/7603 Input/Output System as it is used with the IBM 7070 System. Illustrations accompany the text. In most cases, the sections, sub-sections, and items contained within this manual, are written so that the preceding information serves as a building block for subsequent study.

Each program controlled operation is discussed in detail and is accompanied by operation flow charts and sequence charts. Major signals, key timings, and logic locations are also provided.

Future engineering changes may cause minor discrepancies in some of the timings given in sequence charts and other charts (signal, timing and location). They should not change the philosophy of the operations unless the changes are of a major nature and constitute revisions to data flow and operation sequence.

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1.0.00 INTRODUCTION

1.1.00 PURPOSE

The 7070 Input/Output System provides the necessary circuitry for the transmission of:

1. Card reader information into the core storage area of the A & P unit.
2. Core storage information to a card punch or printer unit.

1.2.00 PHYSICAL COMPONENTS OF INPUT/OUTPUT SYSTEM

The input/output system consists of the following units: 7600 input/output control unit, 7603 input/output synchronizer unit, 7400 Printer, 7500 Reader and 7550 Punch.

The 7600 input/output control unit contains most of the circuits used in the programming and execution of information transfers to or from the following units: 7150 Console and associated Typewriter, 7400 Printer, 7500 Reader, 7550 Punch, and 7900 Inquiry Station. The magnetic drum and its related circuitry is also located in the 7600.

The 7603 Input/Output Synchronizer Unit contains:

1. The scan matrixes for input and output
2. The timing circuits needed to synchronize the operation of the various input/output devices with the operation of the 7070.

The 7400 Printer is a modified 407 Printer. It operates at 150 lines per minute. Selection of any of the 120 typewheels is accomplished by control panel wiring.

The 7500 Card Reader uses a modified 83 feed and operates at 500 cards per minute. Flexibility in selection of fields is accomplished through control panel wiring.

The 7550 Card Punch uses the same type punch unit as the 537 Punch and operates at 250 cards per minute. Selection of punching areas in the card is accomplished by the wiring of the control panel.

1.3.00 DATA FLOW

1.3.01 Input

Both numeric and alphabetic information can be read into the 7070. The second and third read stations of the 7500 Reader are used to enter alphabetic information. Only the third read is used to enter numeric information.

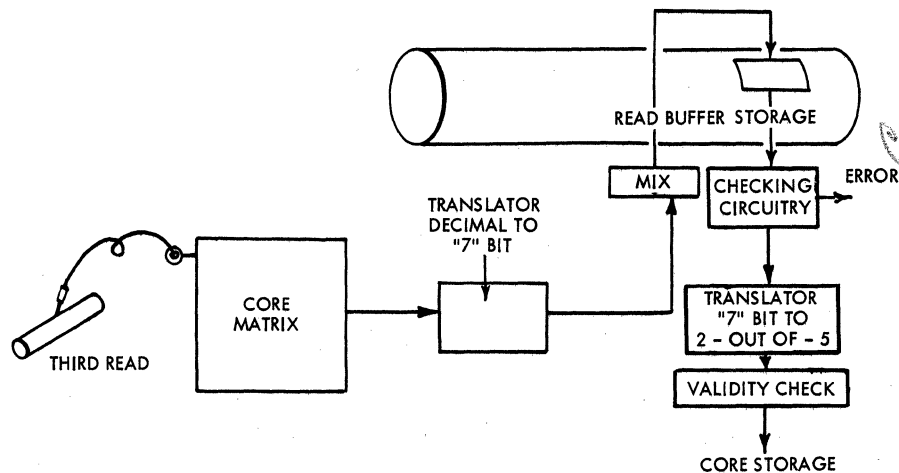


FIGURE 1.3-1 NUMERIC INFORMATION

Numeric Information (Figure 1.3-1)

By means of control panel wiring, the information from the 7500 third read station is transmitted to and stored in a core matrix. The core matrix reads out to a translator and resets before the next digit time.

The information read from the core matrix is translated into the 7-bit coding used in the read buffer storage area. The information is also properly timed so that it is written in the correct area of read buffer storage.

As the information is read from the read buffer storage area of the drum, it is checked for errors. Any error condition signals the A & P unit.

The information read from read buffer storage enters another translator. Here the information is changed from the 7-bit coding used in read buffer storage to the two-out-of-five bit coding used in Core Storage.

After translation, the information is validity checked and transmitted to core storage.

Alphabetic Information (Figure 1.3-2)

As previously stated, both the second and third read stations of the 7500 Reader are used to enter alphabetic information into the 7070. The third read operation is the same as it was when transmitting numeric information, except that all punching 9 through 12 is read.

By means of control panel wiring, the information from the 7500 second read station is transmitted to and stored in a core matrix. The core matrix then reads out to the translator and resets before the next digit time.

The information read from the core matrix is translated into the 6-bit coding used in the read buffer storage prime area. The information is properly timed so that it is written in the correct location in the read buffer storage prime area.

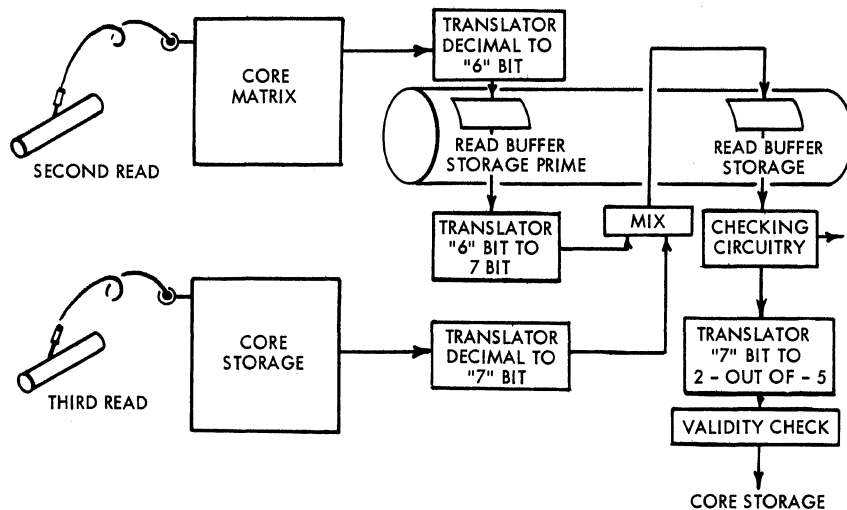


FIGURE 1.3-2 ALPHABETIC INFORMATION

As the information is read from the Read Buffer Storage Prime area of the drum, it is read into a translator. Here the information is changed from the 6-bit coding used in read buffer storage prime to the 7-bit coding used in read buffer storage. The information is properly timed so that it is written in the correct position in the read buffer storage area.

While data is being read from read buffer storage prime and entered into read buffer storage, the same information is also being read from the card at Third Read and entered into read buffer storage. The read buffer storage area now contains duplicate information.

The two duplicate sets of information are read from the read buffer storage area of the drum to the checking circuits. One set of information is matched against the other. Any error sensed signals the condition to the A & P unit.

Translation from 7-bit coding to the two-out-of-five coding is accomplished as previously described under Numeric Operation. The output from the translator is validity checked on the way to core storage.

1.3.02 Output

Both numeric and alphabetic information can be read from the 7070. The information is translated from 7070 type coding into the decimal form used by the various output devices.

Numeric Information (Figure 1.3-3)

Information is read digit by digit from the output buffer storage area of the drum in a two-out-of-five code. The information is checked for validity before entering the translator.

The translator performs two separate operations on the information:

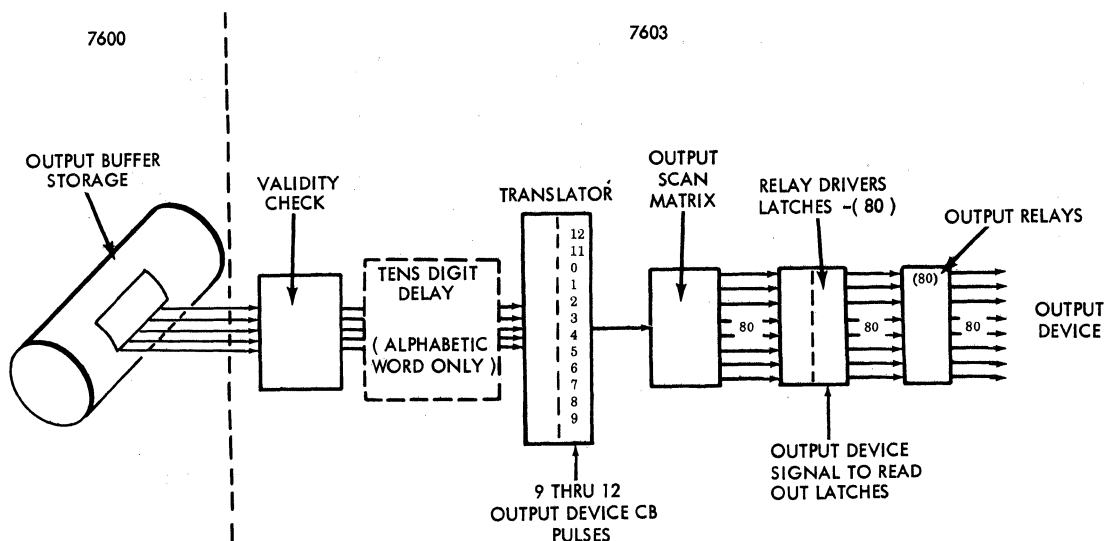


FIGURE 1.3-3 OUTPUT TRANSFER OF INFORMATION

1. It translates the two-out-of-five coding into the decimal coding used by the punch or printer
2. It switches the decimal coded digit with the proper output device circuit breaker pulse. For example, a decimal coded digit 9 switches with a CB pulse which is made at output device 9 time.

The resultant translator output is acted upon by the output scan matrix. The matrix switches the translator output to one of the 80 relay-driver latches.

The relay-driver latch area acts as an assembly and storage area for the arriving pulses. The output device then signals the latches to read out the stored information.

The relay-driver latch outputs pick the output relays and the output relays deliver the pulses to the wired positions of the output device during a particular digit time.

Alphabetic Information (Figure 1.3-3)

Any alphabetic letter stored in the output buffer storage area of the drum occupies two digit positions. The letter is represented by a tens digit and a units digit. The tens digit reads off the drum at odd digit time, and the units digit reads off at even digit time.

To enter the correct relay-driver latch, the tens digit, in its translated form, must reach the latch at the same time as its associated unit digit did. Because the units digit is processed during even digit time, the tens digit is delayed one digit time before entering the translator.

2.0.00 READING CARDS, CIRCUIT DESCRIPTION

Objective: Read data into Core Storage. The following steps are needed:

1. Analyze the instruction + 69, card control.
2. Identify buffer involved and whether operation is input or output.
3. Cause an impulse to the reader clutch provided that:
 - a. The previous card has been completely read (9-12 time).
 - b. The clutch interlock CB in the reader is made.
4. Transfer data from previously read card into core storage from read buffer storage (RBS) via word buffer register. Check for valid data as follows:
 - a. Check each digit position of both alpha and numeric data for two-out-of-five bits.
 - b. Check the alpha data read at the second read brushes against the same alpha data read one reader cycle later at the third read brushes.
5. At end of transfer to Core Storage, interlock to prevent another signal to the reader clutch until after the filling of RBS with card digits 9-12.
6. If data is transferred without error, erase RBS.
7. Transfer RBS' from previous card into RBS.
8. Erase RBS' to get ready for information from next card to be read at second read.
9. At each cycle point, read data from the card into second-read core-row buffer and into third-read core-row buffer.
10. At each cycle point, scan the third-read row buffer into RBS and the second-read row buffer into RBS'.
11. Hold data in RBS until the next + 69 Card Control is developed in the A&P.

Items 3 through 11 are discussed in the material which follows. The remainder is included in Section 5.12, Card Control Operations.

Figure 2.0-1 shows the card input data flow. Note that the following circuit elements are time-shared by the three buffers:

1. Second and third-read core-row buffer drive rings and controls.
2. RBS to word buffer register transfer and checking circuits.

Despite the sharing of these units, all three input machines may operate simultaneously, because each buffer storage area occupies a different sector of the drum.

2.1.00 DATA TRANSMISSION

2.1.01 Second Read (Figures 2.0-1 and 2.1-1)



FIGURE 2.1-1 SECOND READ ENTRY DATA FLOW

2/1/20

PRIME

CHAR.	CARD										RBS					RBS BUFFER STORAGE BITS						G.S. DEC		G.S. UNITS BITS					G.S. TENS BITS					CHAR.							
	12	11	0	1	2	3	4	5	6	7	8	9	A	B	1	3	4	8	A	B	0	1	2	3	6	T	U	0	1	2	3	6	0		1	2	3	6			
A	12			1									A	B	1				A	B	0	1					6	1	0				6	0	1			A			
B	12				2								B	-1	3				A	B	0		2				6	2	0				6	0		2	B				
C	12					3							B		3				A	B	0			3			6	3	0				6	0		3	C				
D	12						4						B			4			A	B		1	3				6	4	0				6		1	3	D				
E	12							5					B	1		4			A	B			2	3			6	5	0				6		2	3	E				
F	12								6				B	-1	3	4			A	B	0						6	6	6	0			6	0		6	F				
G	12									7			B		3	4			A	B		1					6	6	7	0			6		1		6	G			
H	12										8		B				8		A	B			2				6	6	8	0			6		2		6	H			
I	12											9	B	1				8	A	B				3	6		6	9	0			6			3	6	I				
J	11			1									A		1				B	0	1						7	1		1		6	0	1		J					
K	11				2								A		-1	3			B	0		2					7	2		1		6	0		2	K					
L	11					3							A			3			B	0			3				7	3		1		6	0		3	L					
M	11						4						A				4		B		1	3					7	4		1		6		1	3	M					
N	11							5					A		1		4		B			2	3				7	5		1		6		2	3	N					
O	11								6				A		-1	3	4		B	0							6	7	6		1		6	0		6	O				
P	11									7			A			3	4		B		1						6	7	7		1		6		1		6	P			
Q	11										8		A					8	B			2					6	7	8		1		6		2		6	Q			
R	11											9	A		1			8	B				3	6			7	9		1		6			3	6	R				
S		0			2								A	B	-1	3			A		0	2					8	2			2		6	0		2	S				
T		0				3							A	B		3			A		0		3				8	3			2		6	0		3	T				
U		0					4						A	B			4		A			1	3				8	4			2		6		1	3	U				
V		0						5					A	B	1		4		A			2	3				8	5			2		6			2	3	V			
W		0							6				A	B	-1	3	4		A		0						6	8	6			2		6	0		6	W			
X		0								7			A	B		3	4		A			1					6	8	7			2		6		1		6	X		
Y		0									8		A	B				8	A			2					6	8	8			2		6		2		6	Y		
Z		0										9	A	B	1			8	A				3	6			8	9			2		6			3	6	Z			
&	12												B						A	B							2	0	0		2				1	2		&			
—	11												A						B								3	0	0			3			1	2		—			
/		0	1										A	B	1				A		0	1					3	1	0			3		0	1		/				
0			0										A	B					A								9	0				3	6		1	2		0			
1				1											1					0	1						9	1				3	6	0	1		1				
2					2										-1	3				0		2					9	2				3	6	0		2		2			
3						3										3				0			3				9	3				3	6	0			3		3		
4							4										4				1	3					9	4				3	6		1		3		4		
5								5							1		4				2	3					9	5				3	6			2	3		5		
6									6						-1	3	4			0							6	9	6			3	6	0			6		6		
7										7						3	4				1						6	9	7			3	6		1			6		7	
8											8							8			2						6	9	8			3	6			2			6		8
9												9			1								3	6			9	9				3	6			3	6		9		
BL																											0	0			1	2					1	2		BL	
.	12				3						8		B		3			8	A	B	0		2	3	6		1	8	0	1						2		6	.		
\$		11				3						8	A			3		8	B	0		2	3	6		2	8	0		2					2		6	\$			
,			0			3						8	A	B		3		8	A		0		2	3	6		3	8	0			3				2		6	,		
#					3							8				3		8			0		2	3	6		4	8			1	3				2		6	#		
□	12						4					8	B				4	8	A	B		1	2	3	6		1	9	0	1						3	6	□			
*		11						4				8	A				4	8	B			1	2	3	6		2	9	0		2					3	6	*			
%			0						4			8	A	B			4	8	A			1	2	3	6		3	9	0			3					3	6	%		
@										4							4	8				1	2	3	6		4	9			1	3						3	6	@	
+	12																		A																		3	6	+		
-		11																	B																		6	-			

FIGURE 2.1-2 INPUT BUFFER CODING CHART

Core Row Buffer

Read In. The control panel Alpha Pre-Read hubs are wired from the second read brushes. Up to 16 five-character alpha words may be entered from each card. An image of the card row is read into the row buffer at each reader cycle point. Figure 2.1-1 shows the manner in which each core is set. If the corresponding brush is made through the hole in the card, the electronic CB impulse (Figure 2.1-1) sets each core to its one state.

Scan. A Scan Gate Second Read, Buffer 1, is developed during S1 of each card reader cycle point to cause the transfer of the row buffer contents to RBS' drum storage. The cores are sampled in a serial fashion by switching the outputs of the digit and word rings with a DP sample gate. The 80 output pulses (maximum) leave the core buffer serially on the sense line with the D5, W1 core output leaving first in time.

Second Read CB Translator

At each reader cycle point, the pulses coming from the core buffer must be coded into the RBS' code shown in Figure 2.1-2. The six bits of the RBS' code are written in three tracks on the drum as shown in Figure 2.0-1. A, B, 8 are written first; and 1, 3, 4 during the next following digit time.

Figure 2.1-3 shows the bits which must be written at each card-digit time. Note that the one bit may be considered either + or -. A study of Figure 2.1-3 shows that at each reader cycle point except 9, all the bits representing a particular punch may be entered at the same drum digit time (i.e., either early or late).

Further examination of Figure 2.1-3 shows that at card times seven through one, all bits are scanned at late digit time. This is accomplished by the development

↑
 CB
 TIME
 ↓

Card Code	Odd Early			Even Late		
	A	B	8	1	3	4
12		1				
11	1					
0	1	1				
1				1		
2				1	1	
3					1	
4						1
5				1		1
6				1	1	1
7					1	1
8			1			
9			1	1		
1 digit time - 4 u sec	A	B	8	} One Alpha Character		
1 digit time - 4 u sec	1	3	4			

FIGURE 2.1-3 RBS' CODE TIMING

of core sample pulses which result in late time data gates (even-digit drum time) entering the CB translator. As shown in the 2nd Read CB Xlator section of Figure 2.1-1, the late (even-digit) output of second-read core-out switches with CB time 6, 5, 2, 1 to result in a late time output on the A-1 line. This corresponds to the 1-bit entry required as shown on Figure 2.1-3. Similarly, the late output switches with CB time 7, 6, 3, 2 to result in a late time, 3-bit, output on the B-3 line.

In a similar manner, at all card times except 7-1, all bits are scanned so that early-time data gates (odd-digit drum time) enter the CB translator. As shown in Figure 2.1-1, the early-time data gate output of second-read core-out switches with CB time 11 and 0 result in an early-time output on the A-1 line. Similarly, B-bits are entered early at 12, 0 card time, and 8-bits are entered early at 9 and 8 CB time.

The only exception to the translator operation just above is in the entry of bits at 9 CB time. Figure 2.1-3 shows that the 8-bit must be entered early, and the 1-bit must be entered late. The core is scanned in the usual way at 9 CB time to result in an early translator output on the 8-4 line (Figure 2.1-1). The same pulse-out of second-read core-out switches with 9 CB time to turn on delay latch. The delay latch output of late (even) time results in a 1-bit on the A-1 line (Figure 2.1-1).

Alpha characters are formed in RBS' by inserting the numeric portion of the character as the scan is made of the 9-1 punches in the card. The correct combination of AB-bits is then added to form the alpha coded character, when the 12, 11 and 0 punches in the card are scanned (Figure 2.1-2).

RBS' Transfer to RBS

Just before the reader clutch is engaged, information from the card just read at second read is transferred to RBS and RBS' is erased to accept information from the following card. Figure 2.0-1 shows the data flow path needed to accomplish the transfer from RBS' to RBS. The AB 8 (early) portion of each character must be delayed for one digit time so that any combination of bits of a single character enters the 6 to 7 translator at the same time. The 6-bit code of RBS' is translated to the 7-bit code of RBS in the translator. The output is then inverted before entering RBS so that the inverted RBS' characters may later be compared with the true, non-inverted, character read from third read.

For example, consider the entry of the letter F. From the coding summary (Figure 2.1-2) the letter F is coded as:

A	B	0	1	2	3	6	RBS
X	X	X				X	RBS Code for F

when it is entered from Third Read. To be passed as correct by the check circuits when it is read from RBS, the following bits must be entered from the 6-7 translator output:

A	B	0	1	2	3	6	RBS Code
			X	X	X		Inverted RBS code for F

Thus, the RBS' coding for an F, (B, 1, 3, 4) must be translated to the inverted RBS coding for an F (1, 2, 3).

Alpha wds differ from Num.

1. Vdr RBS to WBR.
2. xfer RBS' to RBS
3. Scan 3rd Rd

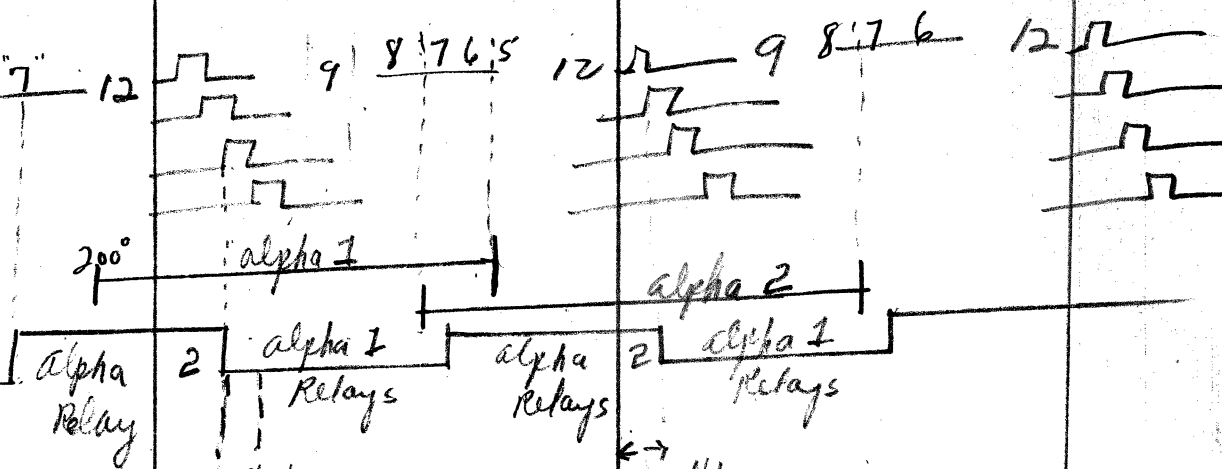
alpha ctrl 1

xfer to G.S.
Erase RBS
xfer RBS' to RBS
erase RBS'

Alpha 2nd Rd
Num. 3rd Rd

Alpha 2nd Rd
Num. 2nd Rd.

all Num.



Alpha core
could flip 16 times
RBS' to RBS
(Sector 1)

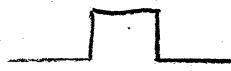
could flip
16 times to
control
RBS - GS.

9 — 12 time
alpha core could
flip 16 times per
CB time for
Scan 3rd Rd.

After RBS to RBS

D1 D0 X 5 9 8 7 6 5 4 3 2 1 0

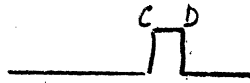
Drum output



'B' Delay



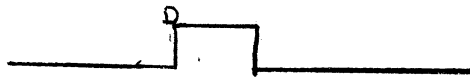
And ckt gate



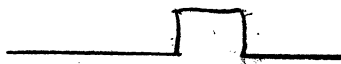
output latch Reset



output latch



output to drum



Wr. Sample



↑
Wr on
Drum

Num wd size of 11 | wd 0 | wd 1

3 2 1 0 | X S 9 8 7 6 5 4 3 2 1 0 | X

Scan Gate 3rd Rd.

WSB Rd. out

WSB 11

Ring START or Sample
cores 0

Ring Run

Advance units Ring
Sample cores

Data trigger

output latch

wd Size of 4

Scan Gate 3rd Rd.

WSB 4

WSB 11

Sample cores D

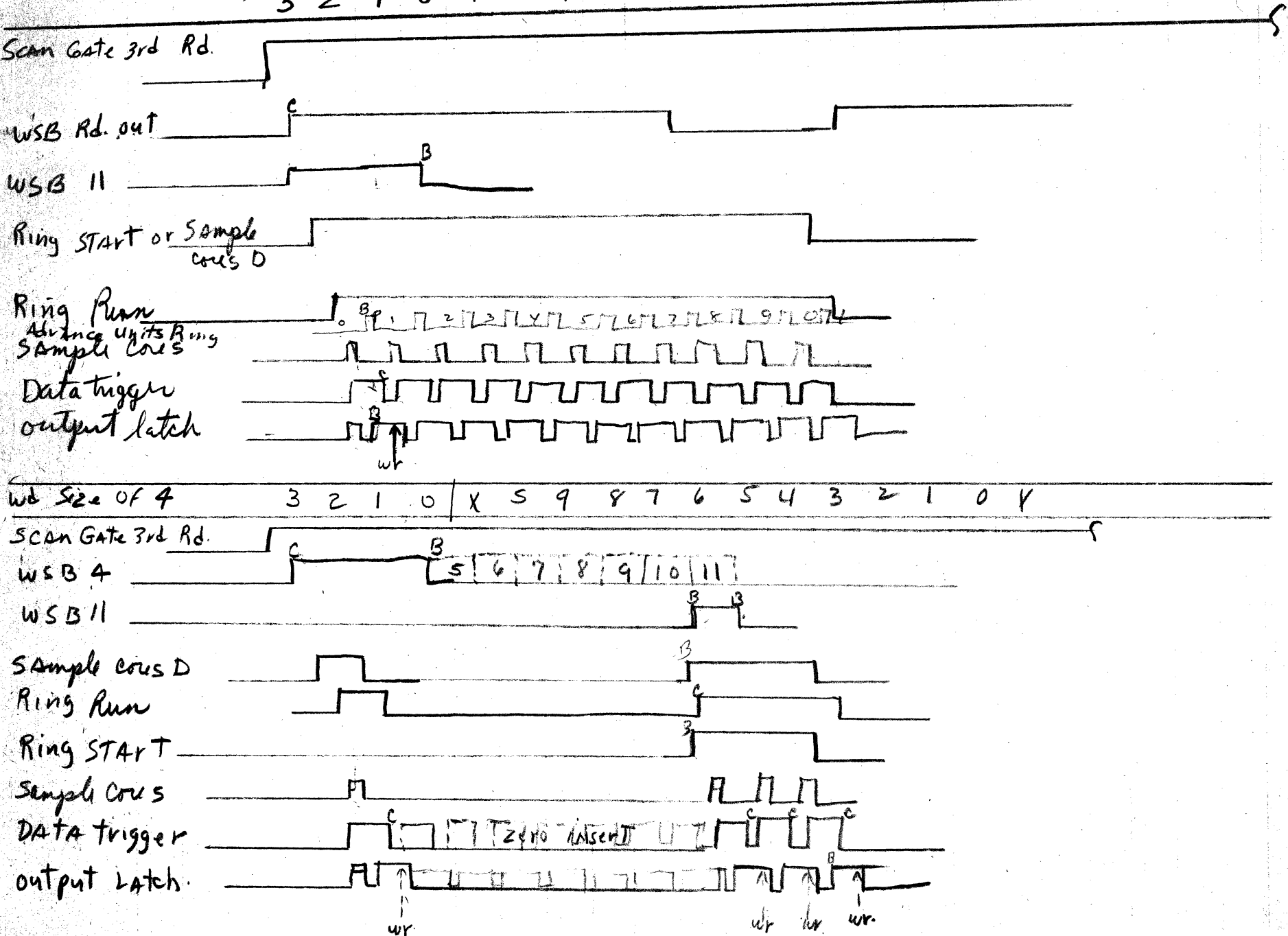
Ring Run

Ring START

Sample cores

Data trigger

output latch



5 CB time
writing GAI Drum.

Wd 0 | Wd I
D4 3 2 1 0 X 5 9 8 7 6 5 4 3 2 1 0

Scan Gate 2nd Rd.

Eu AB, odd Dp

Core Sample

Reset ctrl "on"

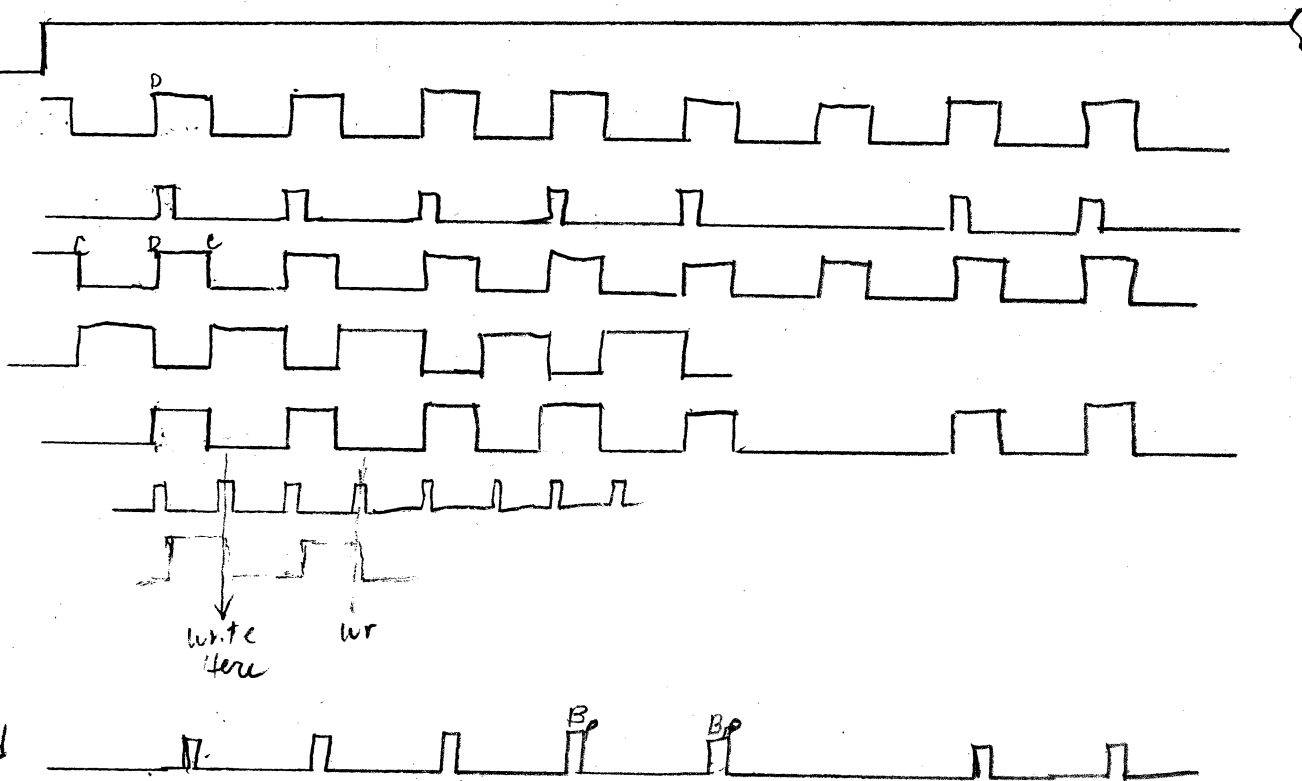
Reset ctrl "off"

2nd Rd Core out

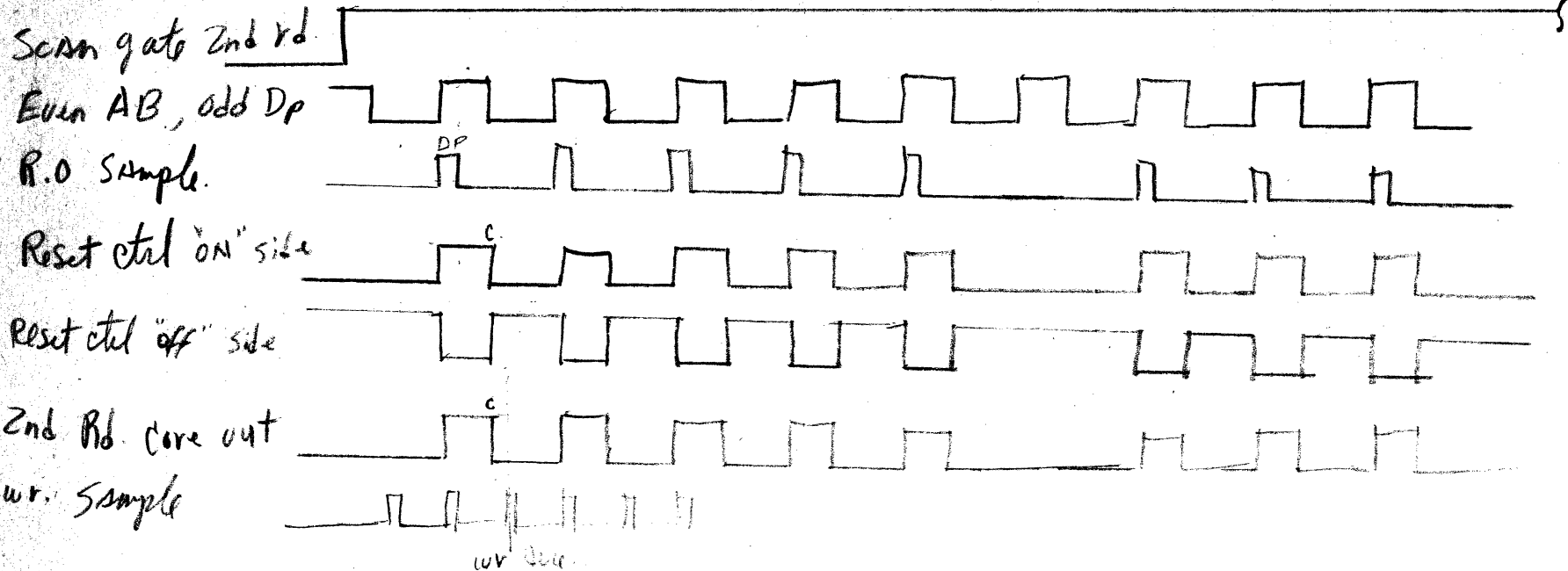
write Sample

output to drum

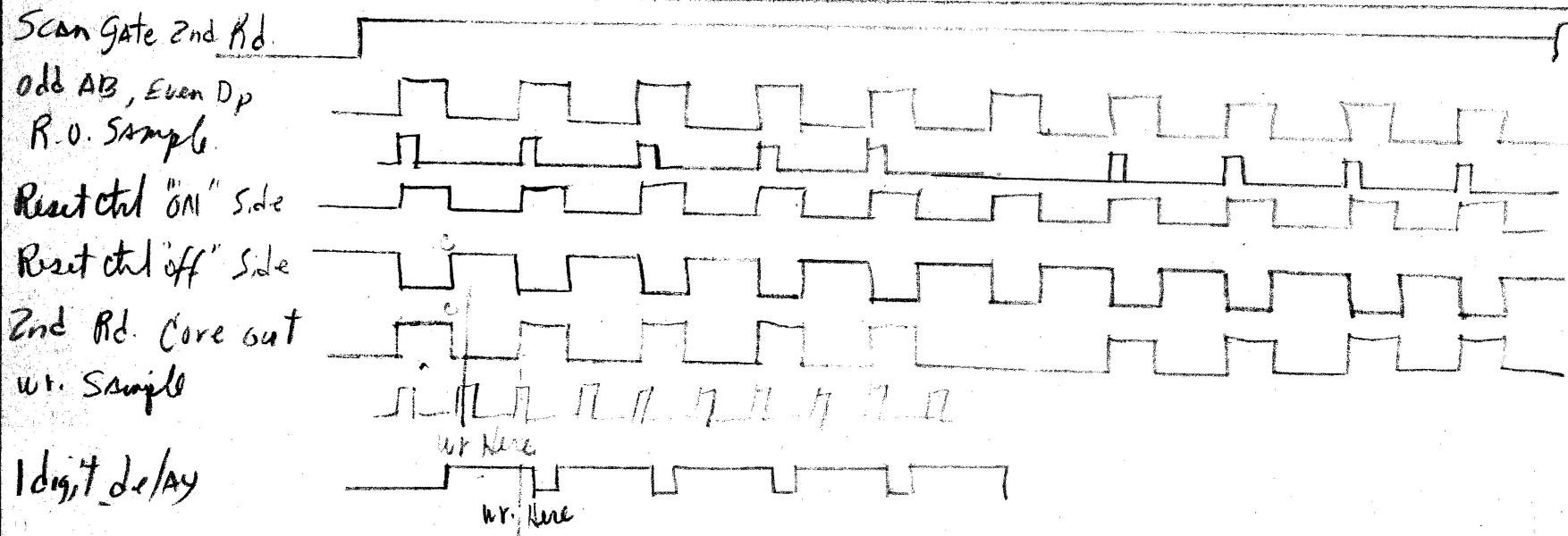
Drive pulses 2nd Rd
digit Ring

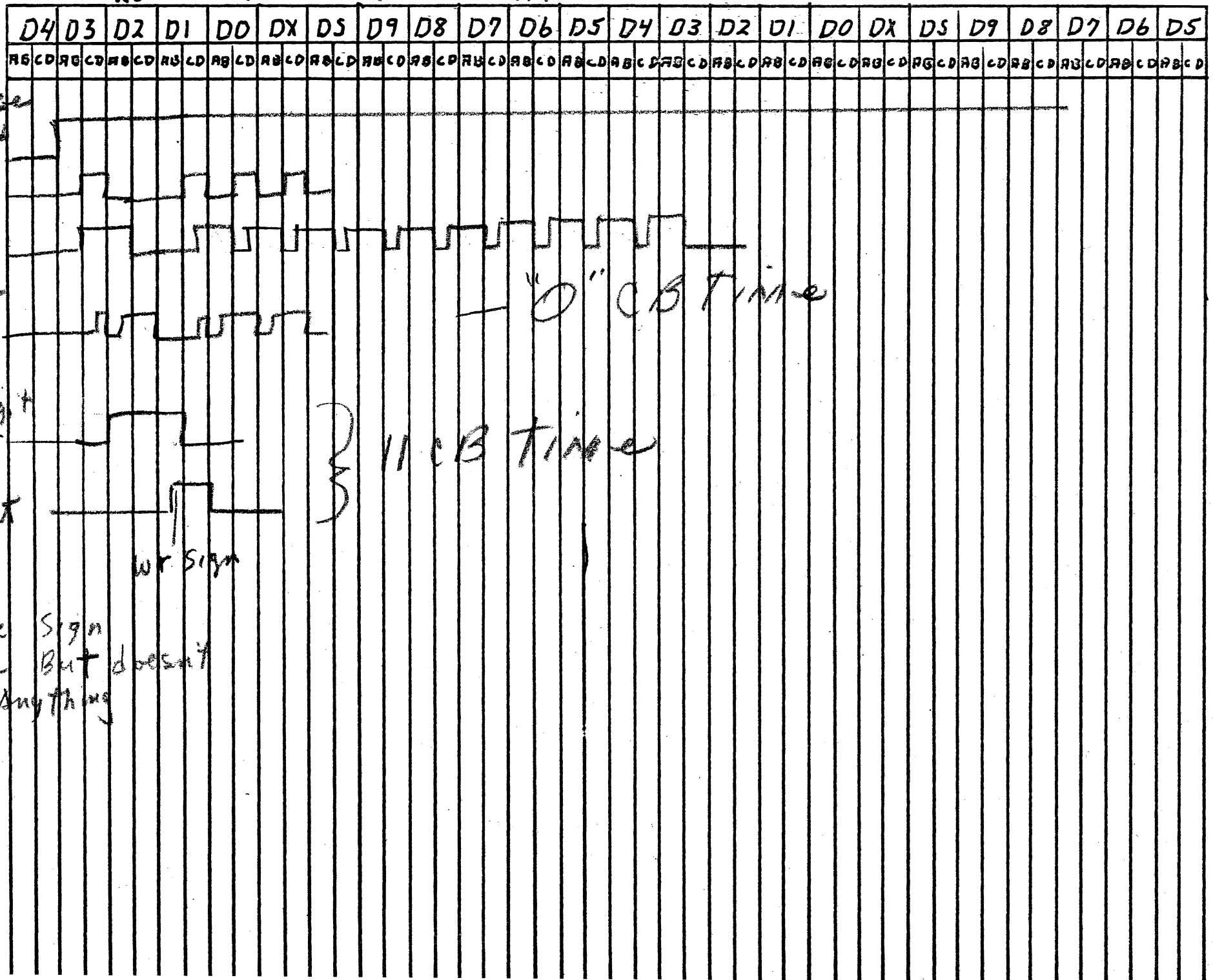


7 CB TIME ^{num} D4 3 2 1 0 | X S 9 8 ^{wa 1} 7 6 5 4 3 2 1 0 | X S



9 CB TIME ^{num} D4 3 2 1 0 X S 9 8 7 6 5 4 3 2 1 0 X S 9





1. Sample Cues
 2. Advance Rings
- Because of wd size wiring

Fig. 2.1-1

wd size wiring

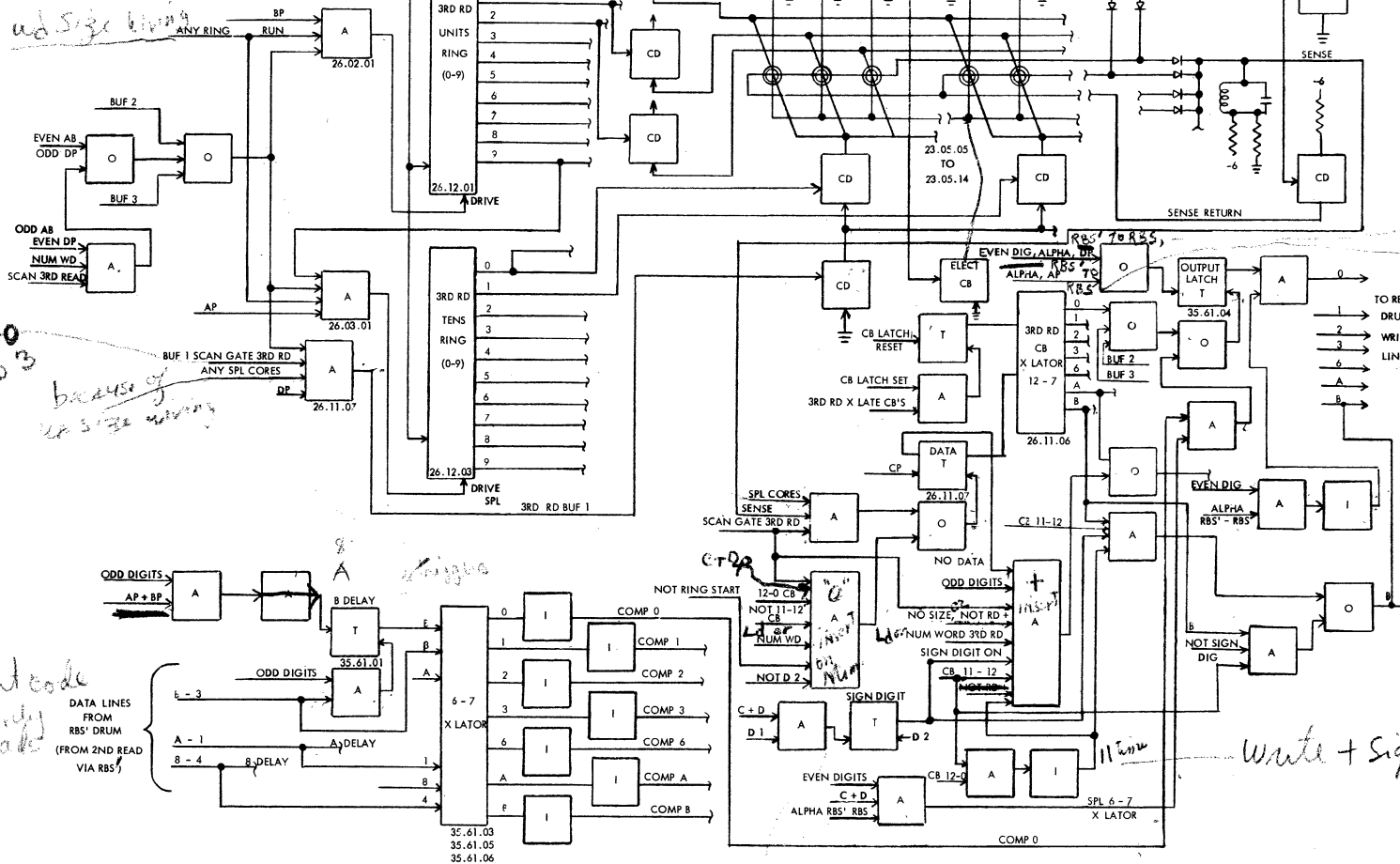


FIGURE 2.1-4 RBS ENTRY DATA FLOW

Digit Delay. The 1 digit time delay is accomplished as shown on Figure 2.1-4 by switching the early, odd digit, AB 8 output of RBS' with odd-digit gates to turn on a delay latch. The latch remains on during AB time of the next even digit. The A, B, 8-bits thus enter the 6-7 translator at the same time as the 1, 3, 4 bits of the same character.

6 to 7 Translator. A positive logic summary of the 6-7 translator is shown in Figure 2.1-5. The RBS code is first translated into decimal form, 1 through 9 and 8/3 8/4. These decimal code lines are next OR'ed together to inhibit the output latches in accordance with the RBS coding requirements shown in Figure 2.1-2. Note that the Sample 6-7 Translator signal on Figure 2.1-4 will cause the entry of bits unless the corresponding inverter is operated. For example, note on Figure 2.1-2 that the 0-bit for card digits 0, 1, 2, 3, 6 and 8-3 must be inhibited. Similarly, the 1-bit for 1, 4, 7, and 8-4 must be inhibited. The switching shown diagrammatically on Figure 2.1-5 follows the same pattern.

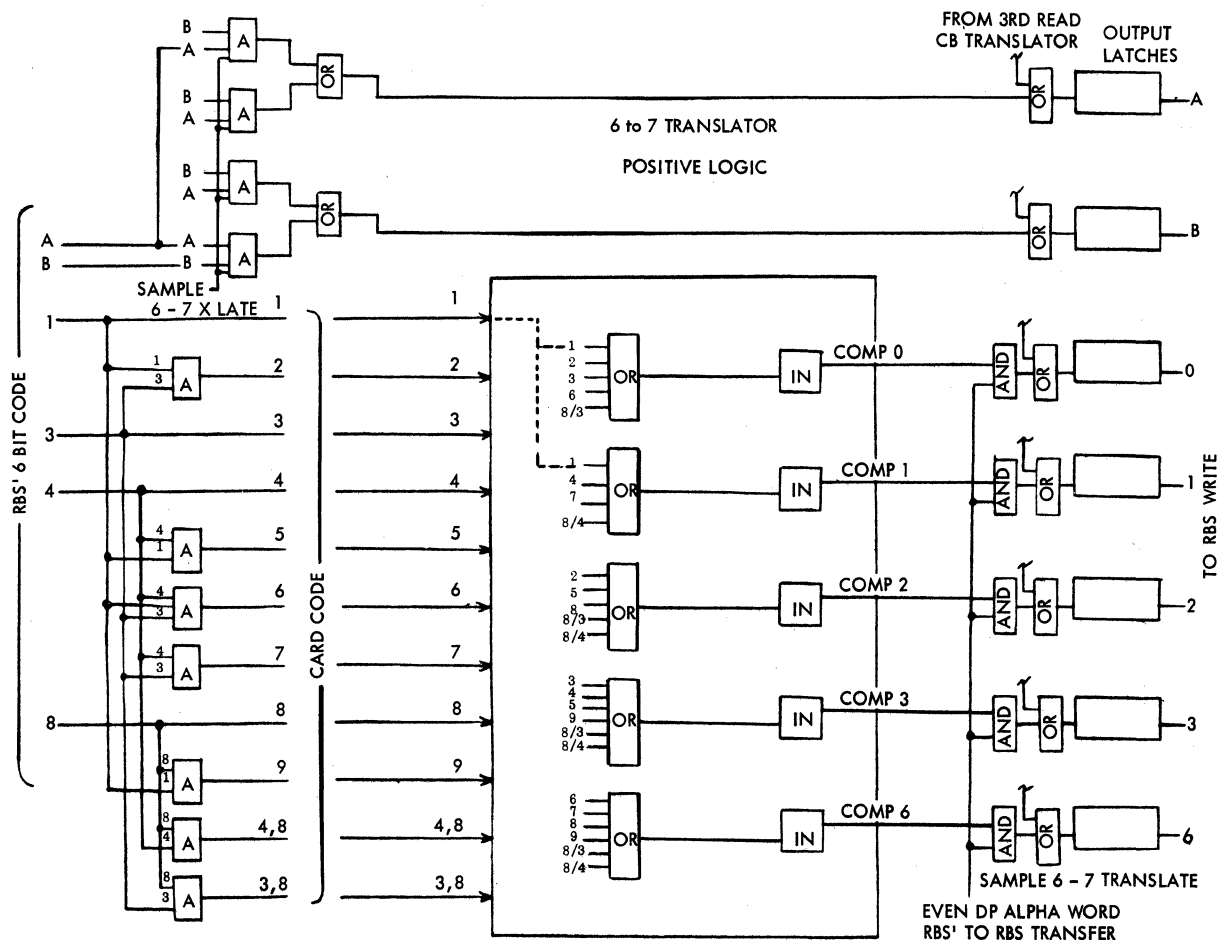


FIGURE 2.1-5 6 TO 7 TRANSLATOR POSITIVE LOGIC

2.1.02 Third Read (Figures 2.0-1 and 2.1-4)

Core Row Buffer

Read In. The third read brushes on the control panel are wired to the storage entry hubs. Words may be of any length from 2 to 11 digits including the sign. The sign must either be punched in a separate column or a column split must be wired to

separate the sign from the numeric punch. Signs are entered to the left of the high-order digit of the word. The operator must also wire Word Exit to Word Size Entry on the control panel to specify word size for any of the sixteen words which are wired. The digit and word rings which scan the core-row buffer advance only as far as the operator indicates with the word size circuits. If 21 digits including sign are being entered, the operator must wire the Exit hub to the U-1 and T-2 Entry End hubs. If the number of digits read in does not agree with the Entry End wired, a third read ring error stop occurs.

Setting of the core at third read takes place in the same manner as at second read when the master CB makes and causes the gating of the electronic CB. See the 7070 Reference Manual, Form A24-7003, for CP wiring examples.

Scan. A Scan Gate Third Read, Buffer 1, is developed after the row buffer cores are set during drum S1 of each reader cycle point. This switches with ring run, sample cores and drum timing pulses. Ring run and sample cores are developed from the control-panel word-size wiring. The only cores that are scanned are those which the operator wires to scan.

Third Read CB Translator (Figure 2.1-4)

At each reader cycle point, the DP bits coming from the third read row buffer turn on the data latch which remains on during AB time. This AB Data latch output is sampled each cycle point by the Third Read CB translator to turn on output latches corresponding to the RBS drum code. The CB translator is wired in accordance with Figure 2.1-2 to produce the RBS code. For example, 6 bits are entered at Reader CB time 9, 8, 7, 6 by switching cams 9, 8, 7, 6 with the data latch output. Similarly, 3 bits are entered at 9, 5, 4, 3 CB time.

Output Latches to RBS

The output latches are on as follows:

- a. Numeric words: even and odd-digit times.
- b. Alpha words: even, AB time with third read data; odd, AB time with RBS' data.

2.1.03 RBS to Core Storage Transfer

Data coming from RBS is handled differently depending upon whether the word is alpha or numeric (Figure 2.1-6).

Numeric

The data follows a path through the check latches and units portion of the 7-2/5 translator to the output latches.

No checking is done by the check latch. The Alpha RBS to GS line is down and the RBS vs RBS' error latch cannot be turned on.

No translation of the code is needed. When Alpha RBS to GS is off, the 0, 1, 2, 3, 6 portion of the RBS code is sampled to turn on the appropriate output latches.

num output - 15 bits
 num. xfer dig. X
 alpha - digit sign

1st Bits off
 RBS come from
 3rd info. then ind
 read inf.

will gate info to xlator on num. info

must get time
 one of these
 A's checks

validity check intended
 See F23

not alpha
 RBS
 40
 D.O
 Section 1

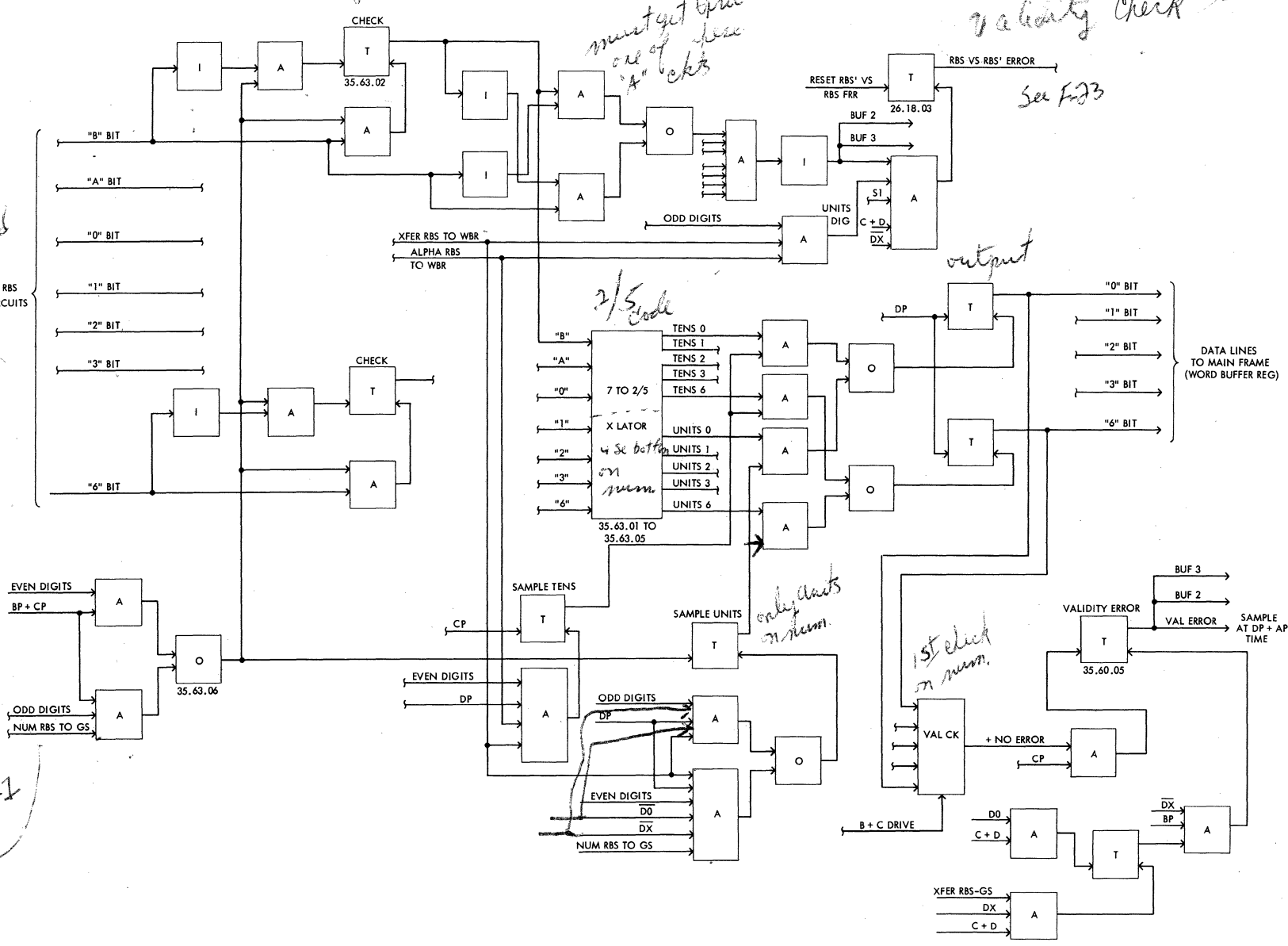


FIGURE 2.1-6 RBS TO GS DATA FLOW

Alphabetic

Checking RBS' vs RBS. The inverted alpha character from RBS' is checked against the true character from RBS at the check latches. Two conditions are valid as follows:

1. A bit at even-digit time may be followed by no bit at odd-digit time. The check latch (Figure 2.1-6) is turned on as shown in the sequence chart (Figure 2.1-7). A check is made at odd-digit time for check latch on and data line down.
2. No bit at even-digit time may be followed by a bit at odd-digit time. The check latch is not turned on. The odd-digit-time check must find the check latch off and a pulse on the data line.

Conditions other than those just listed cause the RBS vs RBS' error latch to come on.

7 to 2/5 Translator. As shown in the sequence chart (Figure 2.1-7), data from RBS at even-digit time turns on the check latch. The latch output enters the 7 to 2/5 translator where it is sampled twice, once for the entry of the tens digit and once for the entry of the units digit of the alpha general storage code.

1. Units Translation. A study of Figure 2.1-2 shows that the 0,1,2,3,6 bits from RBS are identical to the core storage units bits except for characters &, -, zero, and all 8-3, 8-4 special characters.
2. Tens Translation. The tens bits required for the entry of each character can be seen from Figure 2.1-2. The key switching needed to enter each tens bit for alpha characters is shown in Figure 2.1-8.

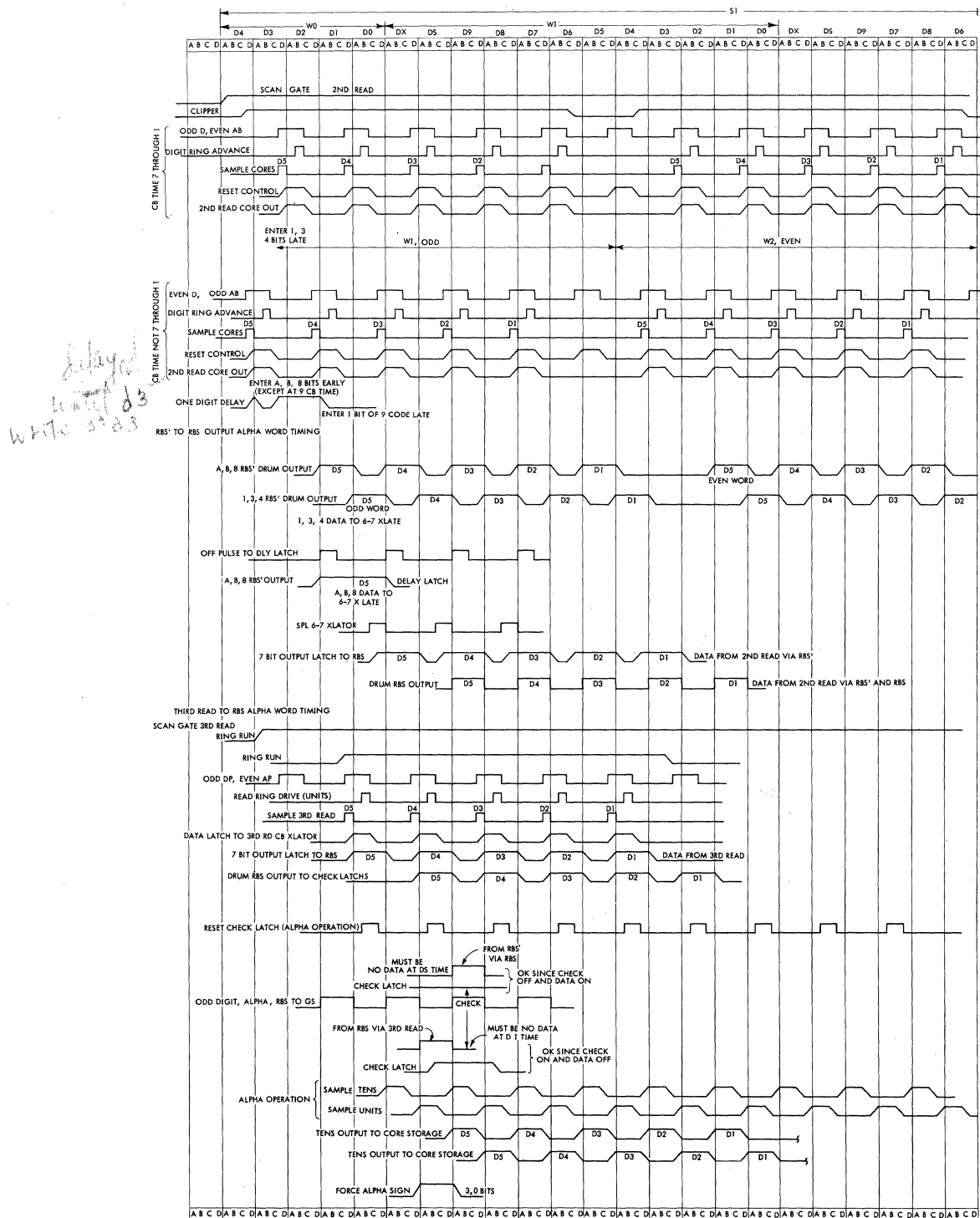


FIGURE 2.1-7 SECOND READ TO RBS' ALPHA WORD TIMING

	<u>Logic</u>	<u>Location</u>	<u>Pin</u>	<u>Character Code</u>	<u>Key RBS Signals</u>
0 Bits	35.63.03	5D	H16F	20,30,31,18,28, 38,19,29,39	
		5D	H16E	61 through 69	A + B and No Special Characters
1 Bits	35.63.03	5F	J20F	48 and 49	8-3/8-4 Special Characters No Zone ie $\bar{A} + \bar{B}$
		5F	J20E	18 and 19	8-3/8-4 A + B
		5F	J20D	71 through 79	B + $\bar{A}$ No Special Character
2 Bits	35.63.04	5B	D14D	28 through 29	8-3/8-4, Special Character B $\bar{A}$
		5B	E	20	A + B, No Numeric (0 1 2 3 6)
		5B	F	82 through 89	A + $\bar{B}$, No Special Characters, Numeric (ie 0, 1, 2, 3 or 6 bits)
3 Bits	35.63.04	4F	E14D	31, 38, 39	A + $\bar{B}$, Any Special Character
		4F	E	30	B + $\bar{A}$ No Numeric (0 1 2 3 6)
		4F	F	1 through 9	No Zone, No Special Character, Not Blank
				0	A $\bar{B}$, No Special Character, Not Blank
				48 and 49	No Zone, Special Character
6 Bits	35.63.04	3H	J14D	Alpha and Numeric	Not Blank, No Special Characters

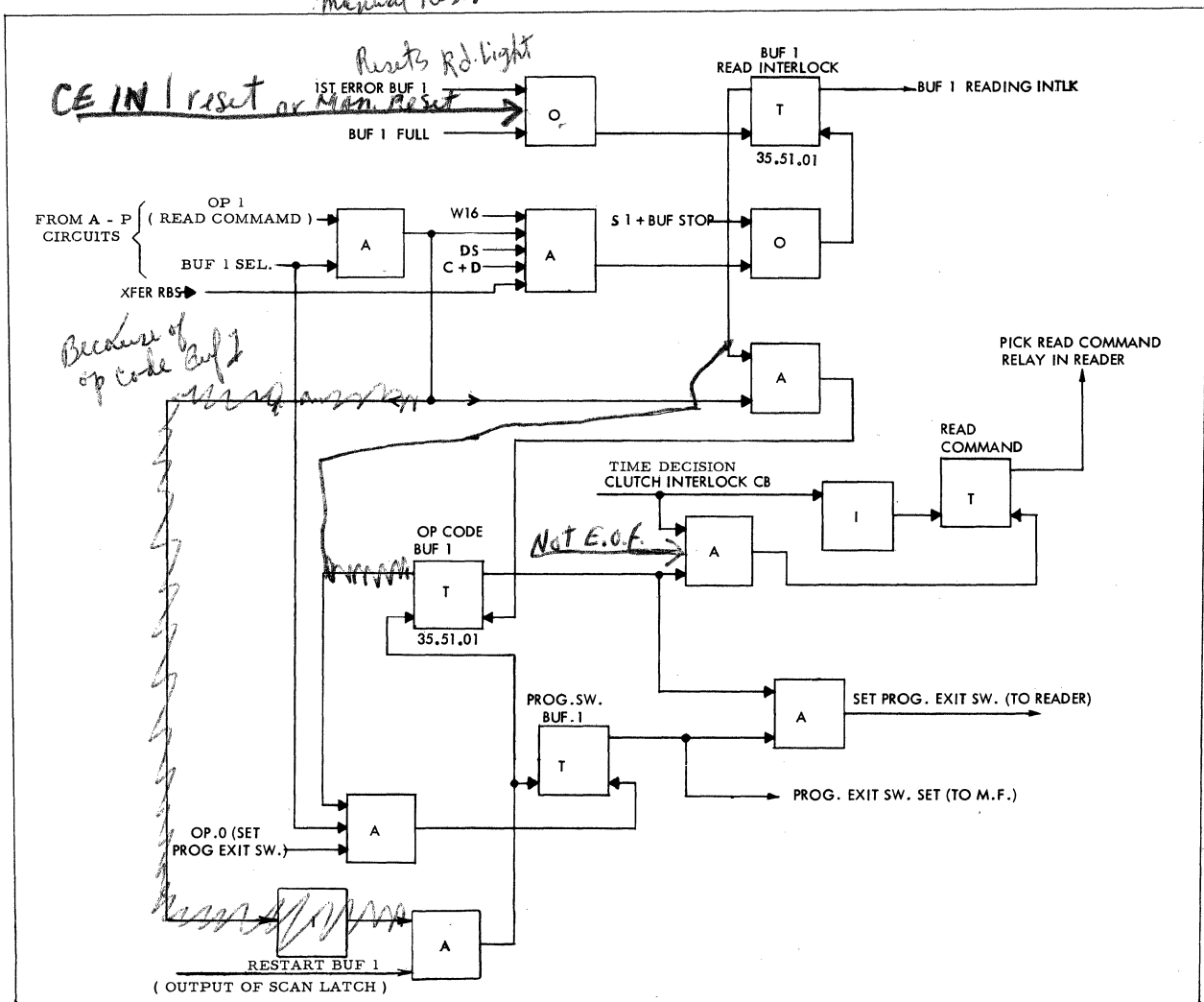
FIGURE 2.1-8 TEN BITS ENTRY SWITCHING

2.2.00 DATA TRANSMISSION CONTROLS (Figures 2.2-1, 2, 3, 4 and Reference Manual, Form A24-7003)

2.2.01 Control Units

Word Exit

Each of the 16 word-exit hubs is tested as the drum revolves through the 16 words of Input Buffer 1. The test impulse is an early word gate which occurs one word early for each word exit. As shown on Figure 2.2-1, the test gate to word exit W1 occurs at S1, W0, D9-D3 time.



Word Size Entry

The 11 word-size-entry hubs accept control panel wired impulses from the word-exit hubs. As the drum revolves through S1, the word-size buffer (WSB) cores are set by one-word-early gates from word exit. Immediately after each core is set, it is read out to turn on the corresponding stage of a trigger ring.

Word Size Buffer Trigger Ring

This ring is started each buffer word time (if appropriate control panel wiring is present) by the D3-D6 time read out of the WSB core. The ring then runs through its eleventh position in the case of a numeric word or through six in the case of an alpha word. At the end of the word-size buffer ring, the third read rings (units and tens) begin advancing to scan the digits of the input word. Thus, the function of the ring is to cause the automatic skipping of the scan of the higher-order digits of a numeric word of less than 11 digits (including sign) or an alpha word of less than five digits.

2.2.02 Second Read to RBS Controls

All information read at the second read station enters the row buffer and RBS' as alpha data if appropriate control panel wiring is present. Even though third-read control-panel wiring is present for non-alpha words, only those words designated as alpha will be checked against the same words read at the third read station.

The first step in reading each row of holes in the card into the core buffer is to cause the electronic CB to operate and thus set each core if the corresponding brush is made through the hole in the card. This is accomplished at each cycle point by the pulse from the 1 ms single shot (Figures 2.1-1 and 2.2-2).

After the setting of the cores has taken place, and the scan gate has been developed (Section 2.4.00), the scan of the row buffer begins. The scan takes place differently depending upon whether the scan is taking place during 7-1 CB time or during other than 7-1 CB time (Figure 2.1-1). The reason for this is discussed in detail in Section 2.1.01. The Second Read RO Gate is developed at Odd DP, Even AB time for 7-1 CB time. This switches with a DP to sample each core and with the next following BP to cause the advance of the second-read digit and word rings. At other than 7 through 1 time, the sample core and ring drive pulses are developed at Even DP, Odd AB time. The timing of this operation is shown in Figure 2.1-7.

2.2.03 Third Read to RBS Controls (Figures 2.1-4 and 2.2-5)

The advance of the third-read ring units and tens, as well as the DP sample gate, is under control of the word-size buffer ring. Two modes of operation are provided as follows.

Numeric

At D2 time during the scan of each word, the ring-run latch is turned on and a sample-cores gate is generated to provide for the sign scan (Figure 2.2-1). Depending upon the word size, the word-size buffer ring runs a variable length of time until the eleventh step is reached. At this point, both sample cores and ring run are turned on to provide for both core sampling and units, tens ring advance. Figure 2.1-4 shows how both ring drive and sample cores are developed at each digit time on a numeric operation. Figure 2.2-5 shows the development of ring run and sample core gates for both 3 and 11-digit numeric words.

Alpha

During the scan of the row buffer at each reader cycle point, a one-word-each early test is made to set the word-size core for the next word to be read in (Figures 2.2-1 and 2.2-8). The same test also checks the alpha relay points for the next word. If the alpha points are transferred, the alpha core is set. The alpha core is read out at the same time as the word-size buffer cores to turn on a alpha word 3rd read latch (Figure 2.2-1). This early-word testing and setting of the alpha core are repeated for each of the 16 input words which are control panel wired to be alpha.

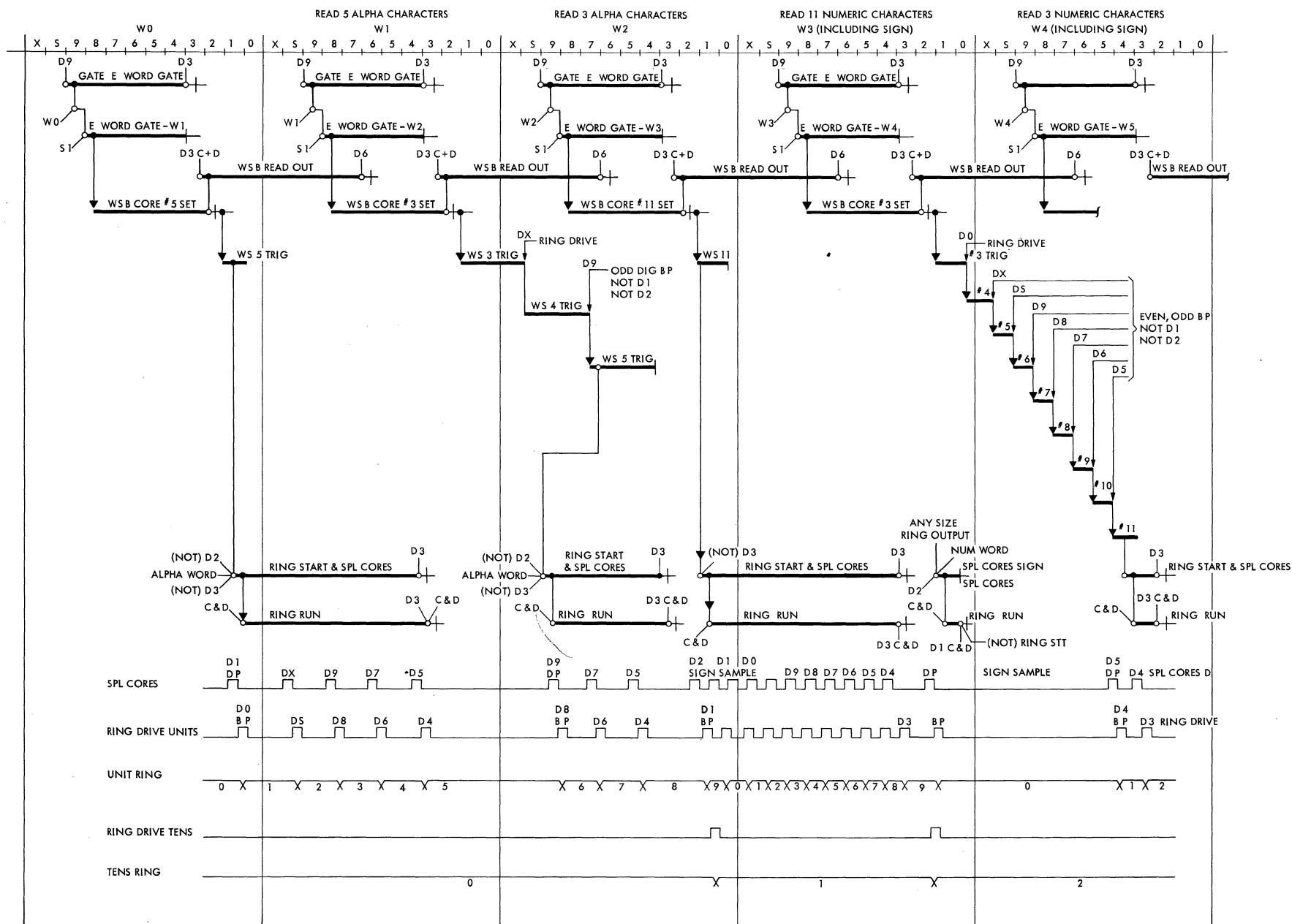


FIGURE 2.2-5 ALPHA NUMERIC READ-IN

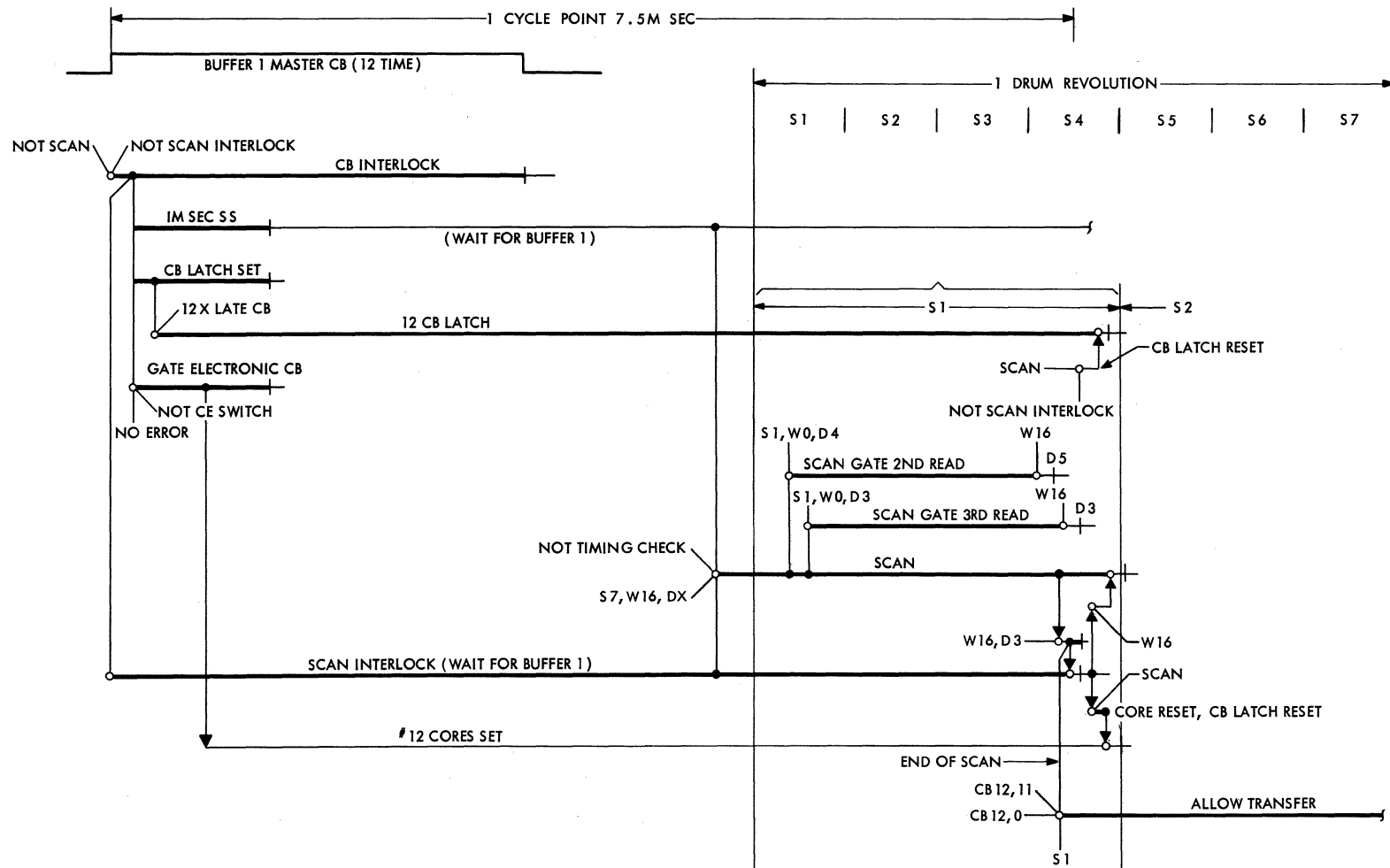


FIGURE 2.2-6 INPUT-READER, DRUM SYNCHRONIZATION

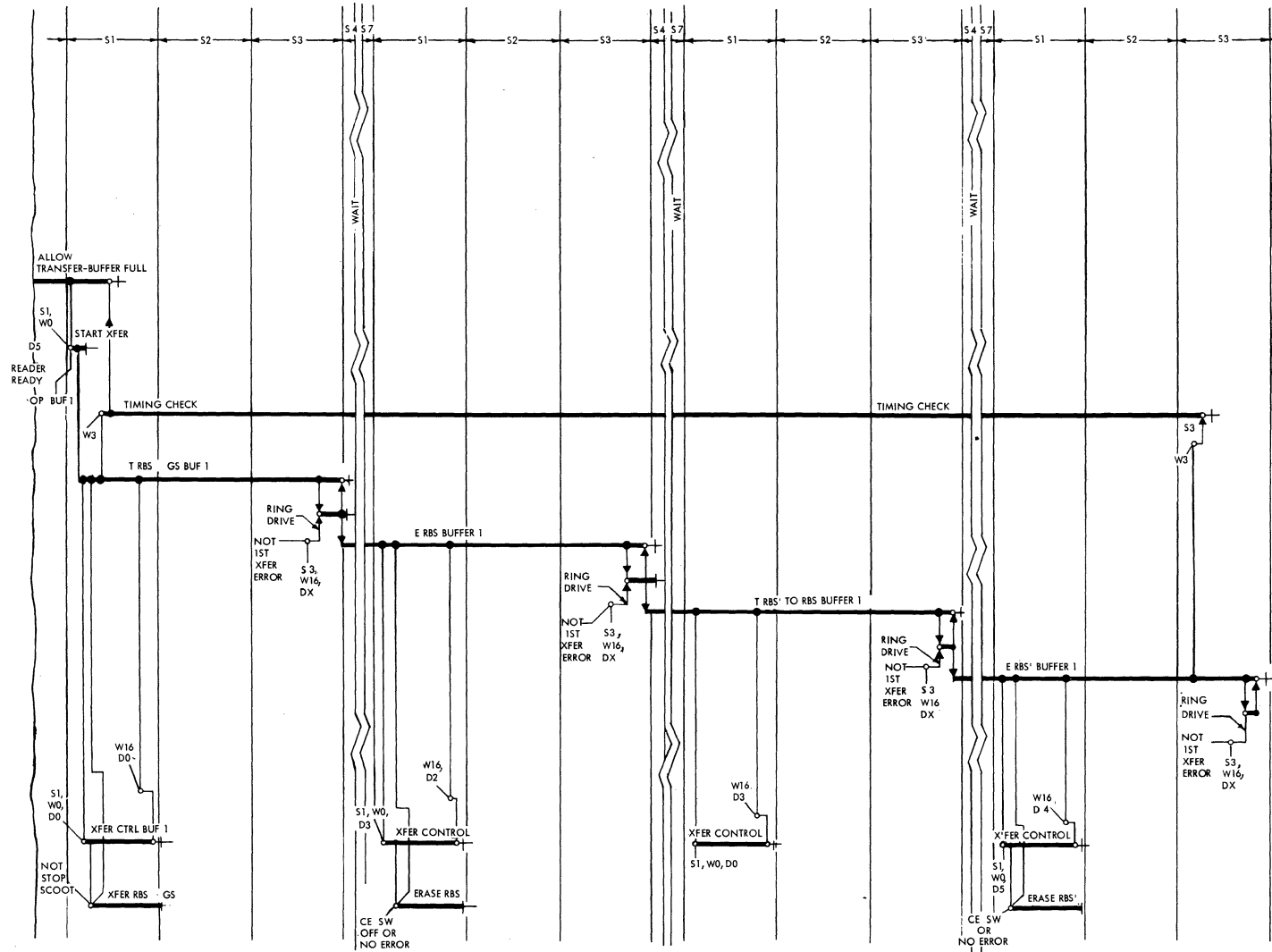


FIGURE 2.2-7 INPUT-READER, DRUM SYNCHRONIZATION

Just before 11 time of each reader cycle (200°), an alpha 1 relay is picked for each input word which is wired to be alpha. The alpha 1 relays must be dropped before 200° of the next cycle so they may be selectively repicked. However, the same alpha indications are needed through 12 time. Thus, a set of alpha 2 relays must be used to hold the alpha 1 indications so alpha 1 may be dropped in preparation for possible repicking. Alpha 1 points cause the pick of the corresponding alpha 2 relay at 20°, just before 7 CB time.

As a result of this transfer of the alpha-word indication from alpha 1 to alpha 2, the one-word-early test must be transferred from alpha 1 points to alpha 2 points during the reader cycle. This is accomplished by the relay-control trigger shown on Figure 2.2-8. Just before 9 reader time, an Erase RBS Buf 1 signal sets the relay-control trigger so that the alpha control 2 relay is picked in the reader. While alpha ctrl 2 is up, (9, 8, 7 time) one-word-early tests are made thru the alpha 1 points.

After the scan of the row buffer at reader cycle point 7, a W16 gate flips the trigger to de-energize alpha ctrl 2 and energize alpha ctrl 1. The alpha ctrl 2 n/c point and alpha ctrl 1 n/o point complete a circuit to the alpha-word core during reader cycle points 6,5,4,.....12.

Just before cycle point 11, the alpha 1 relays may be selectively repicked in preparation for the read-in of the next card. The alpha core can not be set through alpha 1 points at this time because the n/c alpha ctrl 1 point is open and alpha ctrl 2 is down. Similarly, alpha 2 relays hold through D8 time of the following cycle, but the points cannot be used because the n/c alpha ctrl 2 point is open at 9,8, and 7 time.

Because alpha information read at third read must be interspersed in RBS between the alpha data from second read, on alpha words the third read cores are sampled and the units ring is advanced at alternate digit times (Figure 2.1-4). The off side of the alpha word 2rd read latch, also called Numeric Word, (Figure 2.2-1) prevents the sample and ring drive at alternate digit times because it is down for all alpha words.

Figure 2.2-5 indicates the development and timing of sample cores and ring drive pulses for both 3 and 5 character alpha words.

2.2.04 RBS to WBR Controls

The 7070 program may advance to a card control, read instruction, at any time relative to the reader cycle. Figure 2.2-9 shows schematically the pre-sensing of the Card Control Op and the ensuing data request which brings the 1st Record Control Word to the auxiliary register. The Card Control Op Code is now analyzed and an Op 1 (read) signal is sent to the input/output synchronizer. The buffer to be used is also identified with a Buf 1, 2 or 3 Select Signal. The Op 1 and Buffer 1 signals are shown schematically on Figure 2.2-9 and in positive logic form on Figure 2.2-3.

Reader Clutch Energization

The Op 1 and Buf 1 signals are AND-switched (Figure 2.2-3) and then switched with the off side of the Buf 1 Read Interlock latch. This latch is normally turned off by the Buf 1 Full signal from Figure 2.2-2. Buf 1 Full occurs after the

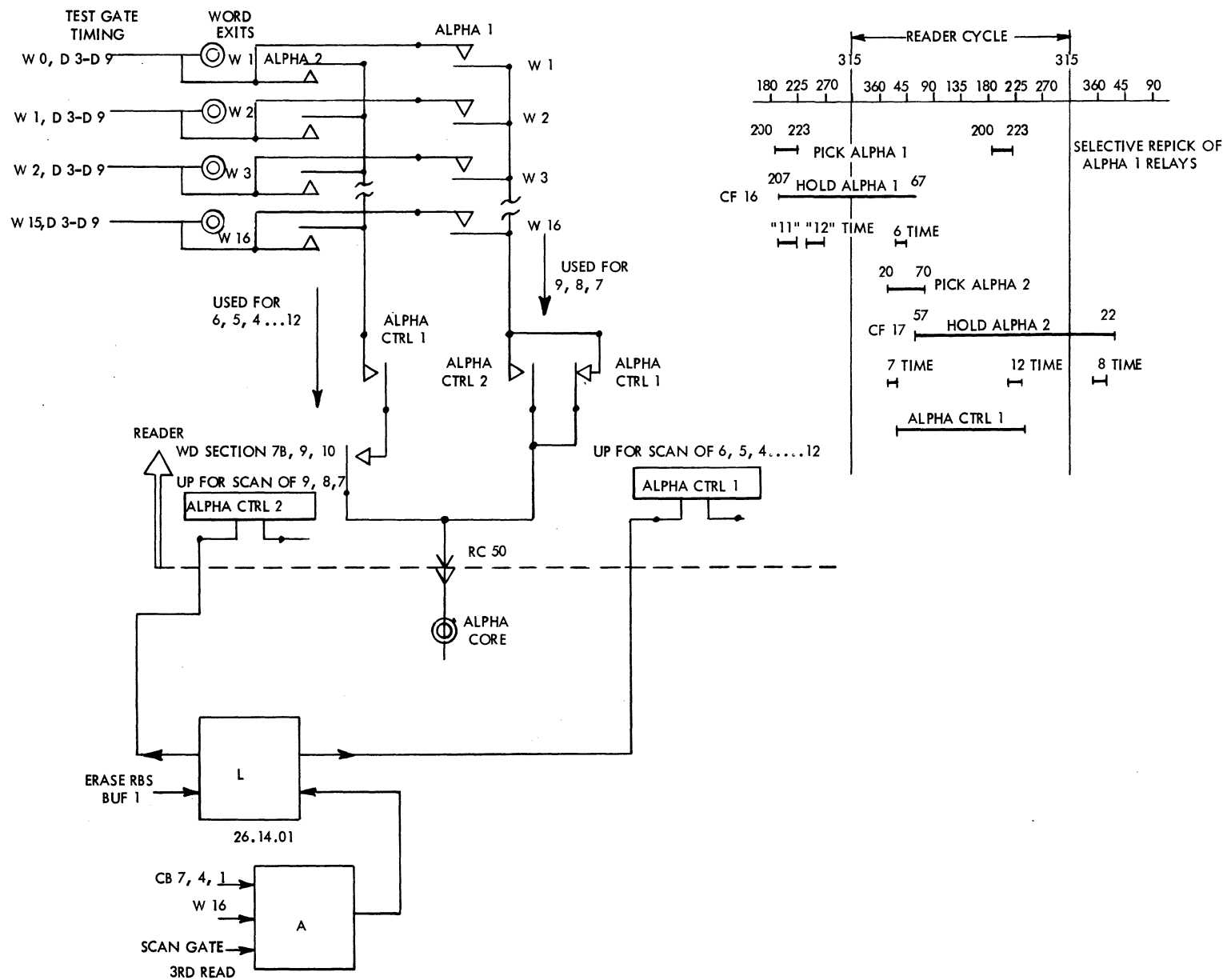


FIGURE 2.2-8 CIRCUIT AND SEQUENCE FOR ALPHA WORD IDENTIFICATION

"12" row buffer cores have been scanned from the previous card. Thus, Op Code Buf 1 is turned on and, if the Decision Time CB is made in the reader, a read-command signal results in the operation of the reader clutch (under CB control). Note that a considerable time delay, relative to a drum revolution, occurs before the reader can move, and the 9's can be read from the next card into the drum buffer. The transfer to storage and erase of drum buffer occurs during this delay.

Transfer RBS to WBR

As shown schematically on Figure 2.2-9 and in positive logic form on Figure 2.2-2, the Op 1, Buf 1 signals cause the start of the transfer and erase ring. Note that if the ring is to be started, cards must be in the reader, the scan of 12's must have been completed, and the drum must be at the beginning of Sector 1 (Buf 1). The first step on the ring, T RBS to WBR Bfr 1 if further switched with a timing gate, X'fer Ctrl Buf 1, and with Not Stop Scoot to cause X'fer RBS to WBR. This causes the read out of the 16 words of RBS to the WBR in the A&P unit if the record control words call for all 16 words. If fewer than 16 words are defined by the record control words, a stop transfer to WBR signal from logic 45.45.62 turns on Stop Scoot (Figure 2.2-2) and the Trans RBS to WBR gate ends.

When the Trans RBS to WBR Gate begins, a W1 DX signal, called DX Start Transfer, is returned to the A&P circuits. This signal starts the program ring and begins the serial read-in to the WBR from RBS. The program ring is recycled at the end of the read in of the first word. The second word is read in from RBS as the first word is being stored in the location specified by the record control words. See 5.12.02 for the card control read operation.

The transfer to WBR operation may end either by the transfer of all 16 words without error or by the A&P circuits sensing the last start address of the last RCW (without error). In either case, 2 one-up instruction-counter operations are performed and an end-data operation signal causes the 7070 program to advance.

Erase RBS

As shown on Figures 2.2-7 and 2.2-9, the transfer and erase ring advances at the next S3, W16, DX, if no error has taken place. The second step on the X'fer and Erase Ring, E RBS, switches with the X'fer Control Buf 1 timing gate to create an Erase RBS gate. Note that if the CE switch (validity check stopswitch) is on and an error (2nd Error) has occurred, the Erase RBS gate is not developed. Thus, when the 7070 stops because of the information-bus validity-check stop, the invalid data is in the RBS to aid in the customer engineer's diagnosis.

Transfer RBS' to RBS

The next step on the X'fer and Erase Ring causes the transfer of the RBS' contents to the just erased RBS.

Erase RBS'

The last step on the X'fer and Erase Ring cause the contents of RBS' to be erased in preparation for reading in the next card from 2nd Read to RBS'. Again, if the CE switch is on, and an error has occurred, RBS' is not erased.

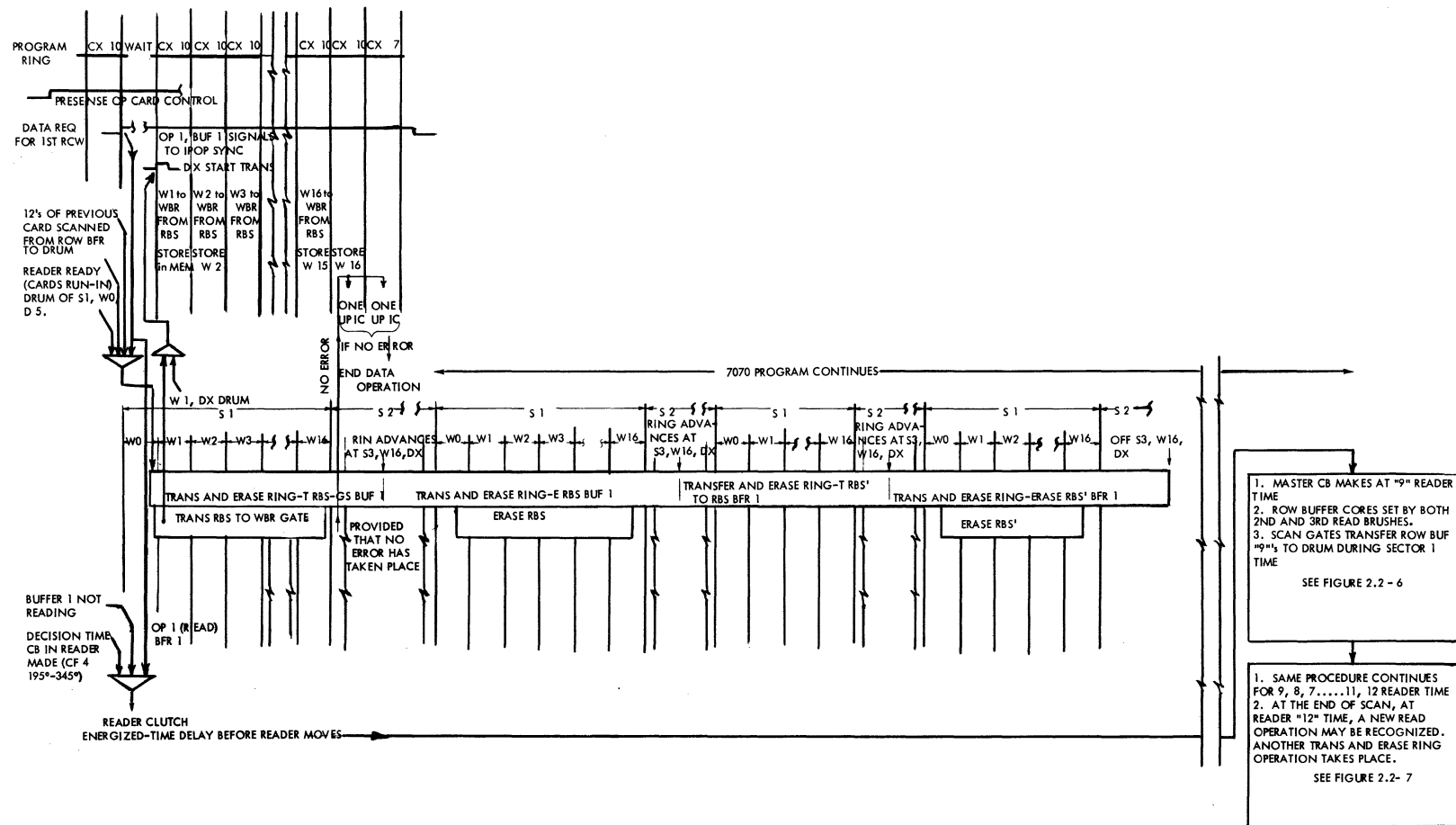


FIGURE 2.2-9 READ OPERATION BLOCK DIAGRAM - NO ERROR

Some time (variable) after the end of the transfer and erase-ring operation, the master CB makes for 9 time, and the two row buffers are set by the second and third read brushes making through 9 holes in the cards. This is shown on Figure 2.2-9 and discussed in section 2.4.00.

2.3.00 SIGN READ-IN OPERATION

2.3.01 Numeric

When the sign is punched in the card and read + is not wired, the sign is read into cores, sampled, and translated to an "A" RBS bit for a + sign and a "B" for a - sign.

On numeric read-in operations when read + is not wired on the control panel, a + sign A-bit must be generated. This is accomplished by switching at the third read CB translator as shown on Figure 2.1-4.

2.3.02 Alpha

The 3, 0 alpha sign is entered by switching a DX C + D sign sample gate with Alpha RBS to GS. This gate is used to force bits on the 0 and 3 lines to core storage at sign time (Logic 35.63.01).

2.4.00 SYNCHRONIZATION TO THE READER

2.4.01 Introduction

At each reader cycle point, an analysis is made at both the second and third read CB translators to determine which bits should be entered in the RBS' and RBS drum buffers. Data flow for this operation is discussed in detail in sections 2.1.01 and 2.1.02. The make of the reader master CB's at each cycle point is synchronized to drum buffer timing by the following circuits.

2.4.02 Sync Circuits (Figure 2.2-2)

As shown on Figure 2.2-2, the make of the reader master CB at each cycle point causes the turn on of the CB interlock latch. This triggers a 1 ms single shot which accomplishes the following:

1. Turn on the scan interlock latch.
2. Sets the translator third-read CB latches for that particular cycle point (See logic 26.11.05): For example, at cycle point 6 Cam 6 3 2 1 and Cam 9 8 7 6 latches are set.
3. Gates the Electronic CB which causes both second and third read core buffers to be set from the brushes.

After the cores are set, they must be scanned during the correct sector time to read into either Buffer 1, 2 or 3. As shown in the operation chart (Figure 2.2-6) for Buffer 1, the scan latch is turned on at the first S7, W16, DX after the end of the 1 ms single shot, if scan interlock has been turned on. The scan latch accomplishes the following:

1. Develops second and third read scan gates.
2. Resets the scan interlock latch at the end of scan
3. Resets the cores in the row buffer in preparation for the next read-in.
4. Resets the particular third read CB latches which were on for that cycle point.
5. Provides a test gate at the end of scan to check for the last cycle point (12) of the card being fed. If all punches in the card have been read into the row buffer and scanned, the allow transfer latch is turned on.

2.5.00 CHECKING CIRCUITS

2.5.01 Ring Check

Third Read Ring Ending Error

The operator must wire the control panel to indicate the total number of positions that the ring is to drive. This is accomplished by wiring the exit hub to the units and tens-entry-end hubs. For example, if 21 digits are to be entered, the tens 2 and units 1 hubs are wired.

The ending of the ring at 21 is checked as shown in Figure 2.2-4 by AND-switching the last ring positions with the entry-end wiring of the control panel. These must agree at W16, D1 of Buffer 1 or the third read ring end error latch is turned on to cause a machine error stop.

Second Read Ring Ending Error

If the second read ring fails to advance through all 80 positions (end at 0, 0), an error is indicated. This condition is checked by turning on a second read rings carry latch when the rings advance to W16, D1 Even (Figure 2.1-1). The next advance pulse moves both rings to their 0, 0 position. The rings-in-error latch is turned on at Buffer 1, W16, D5 time (Figure 2.2-4) if these conditions are not met.

Ring Reset Error

If either second or third read rings are not reset to zero by the W0, D5-D6 ring reset pulse (Figure 2.1-1) the rings-in-error latch is turned on at D5 time (Figure 2.2-4).

2.5.02 Timing Check

The timing error latch shown in Figure 2.2-4 checks for any attempt to read new information into the drum buffer while the transfer and erase ring is in operation. Figure 2.2-7 shows how the timing-check latch is turned on near the beginning of the transfer and erase ring operation and goes off near the end. If CB 9, 8, 7, 6 make during this time, the timing-error latch is turned on, and a machine-error stop occurs.

2.5.03 Validity and RBS' vs RBS Errors on RBS to WBR Transfer

Validity-Check Stop-Switch Off (CE Switch)

When an error occurs, the relation between the card-control operation in the A&P unit and the drum buffer operation is shown in Figure 2.5-1. Circuits are illustrated in Figure 2.2-4. The detection of a RBS' vs RBS error at the check latches or a validity-check error results in an immediate 1st + 2nd Error signal to the A&P unit. This has no immediate effect; however a read-recycle operation is signalled when either of the following conditions occur (Figure 5.12-3):

1. Last word defined by the RCW is reached.
2. Sixteenth word of the drum buffer is transferred to WBR.
3. Any error other than IB Validity Check occurs (Example: RCW Error).

Read recycle signals a data request to read out 1st RCW from storage to the auxiliary register. The usual updating of the IC does not occur because of the error signal.

At the end of Buffer 1, an S2 gate switches with the output of the validity error latch to turn on the transfer-error latch. The normal advance of the transfer and erase ring at S3, W16, DX is prevented from taking place because transfer error is on. The validity-error latch (or RBS' vs RBS) is reset at S3, W2. At the next S1, a second Transfer RBS to WBR gate is developed and a DX start-transfer signal is sent to the A&P circuits. The same series of serial transfers from RBS to WBR is repeated. The WBR to core storage data transfer is done under control of the RCW in the same manner as in the first transfer. Any error which occurs during the second transfer turns either the Val Error or RBS' vs RBS error latch on. The output of either latch switches with S1 and transfer error to turn on second error (Figures 2.2-4 and 2.5-2). If no second error occurs, the IC is updated by two in the usual manner, the transfer-error latch is turned off at S3, W1, and the transfer and erase ring advances at S3, W16, DX.

When an uncorrected error does occur, an end-data operation is signalled without updating the IC by two and a Reset 2nd Error signal is returned to the input/output synchronizer to turn off all error latches. The output of the 2nd Error latch also goes to the reader as a RVC Error signal. At the discretion of the operator, the error card may be offset, or the reader may be stopped. The card following the error card is fed and read into RBS and RBS' whether the error is corrected or not. The invalid information enters the core storage because the IB validity check is prevented from turning on Any Error during a card-control operation (Figure 5.12-3A). Because the program branches to I+1, the programmer can either stop the 7070 program, enter an error routine, or skip the processing of the error card by immediately feeding another card.

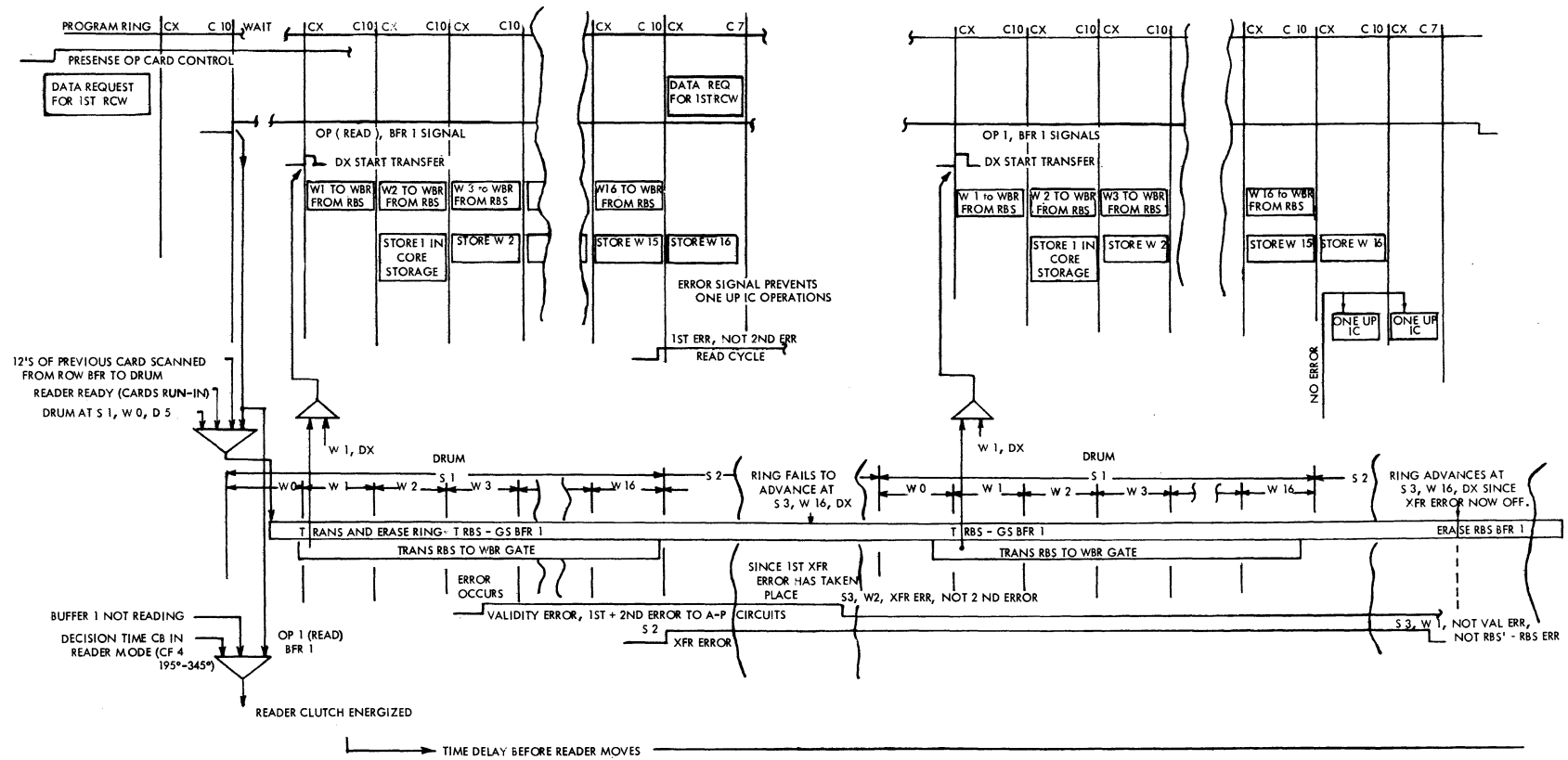


FIGURE 2.5-1 READ OPERATION BLOCK DIAGRAM - ERROR, 2ND TRANSMISSION CORRECT

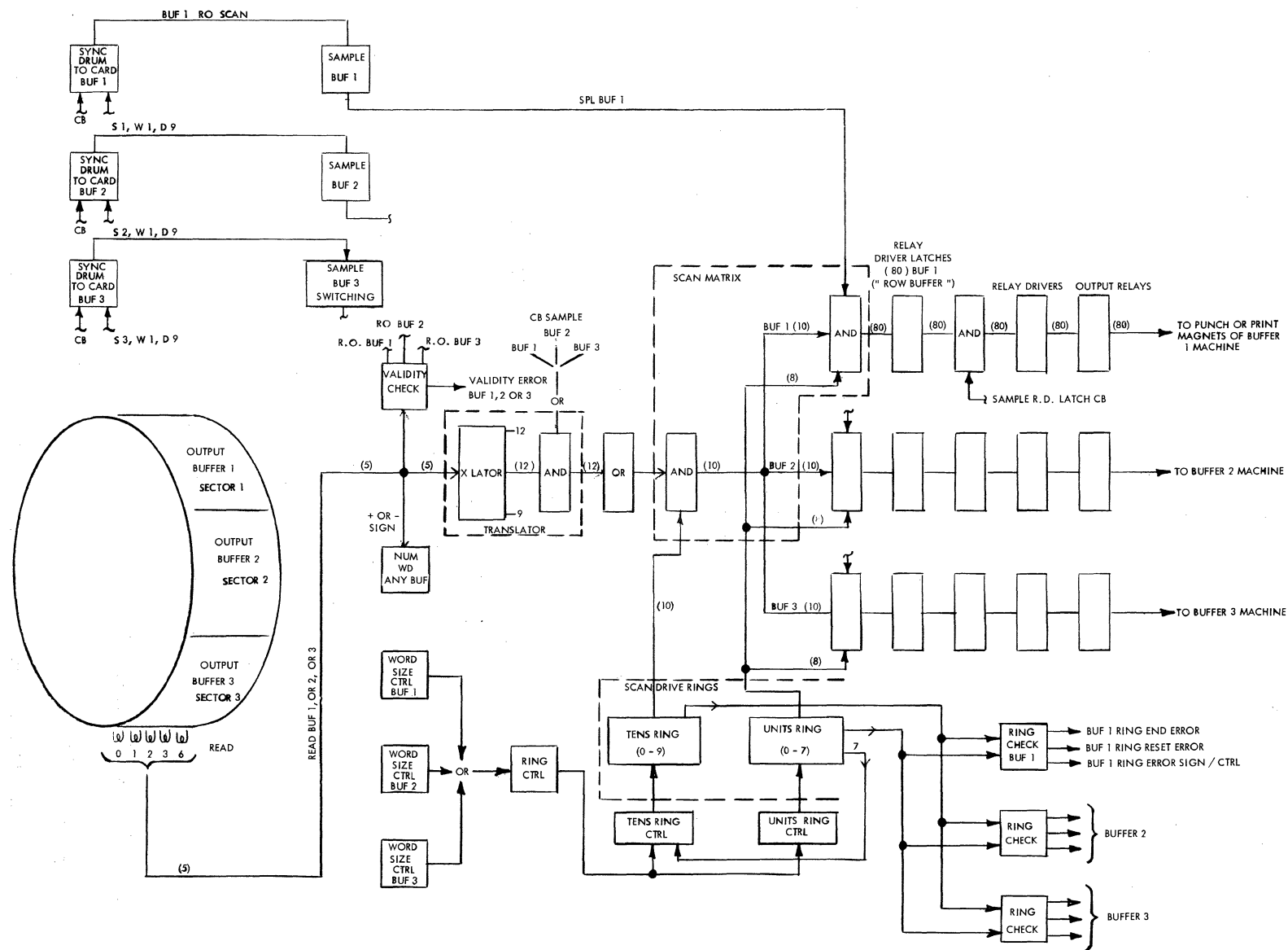


FIGURE 3.0-1 OUTPUT BUFFER DATA FLOW

3.0.00 PUNCHING CARDS, CIRCUIT DESCRIPTION

Objective: Punch data from core storage. The following steps are needed:

1. Analyze the instruction + 69, card control.
2. Transfer data from core storage to the drum output buffer storage.
3. Energize punch clutch.
4. Read data from the drum onto the drum data bus.
5. Check validity of drum output.
6. Translate from the drum 2/5 code to decimal.
7. Scan the translator output to determine the columns to be punched.
8. Operate output relays.
9. Operate punch (or print) magnets in the output machine.

Items 3-9 will be discussed in the material which follows. The remainder will be found in A&P Section 5.12.

Figure 3.0-1 shows the output data flow for a three-buffer machine. The following units are time-shared by all three buffers:

1. Validity check
2. Translator
3. Portion of the scan matrix gated by the tens ring
4. Units and tens ring and ring control

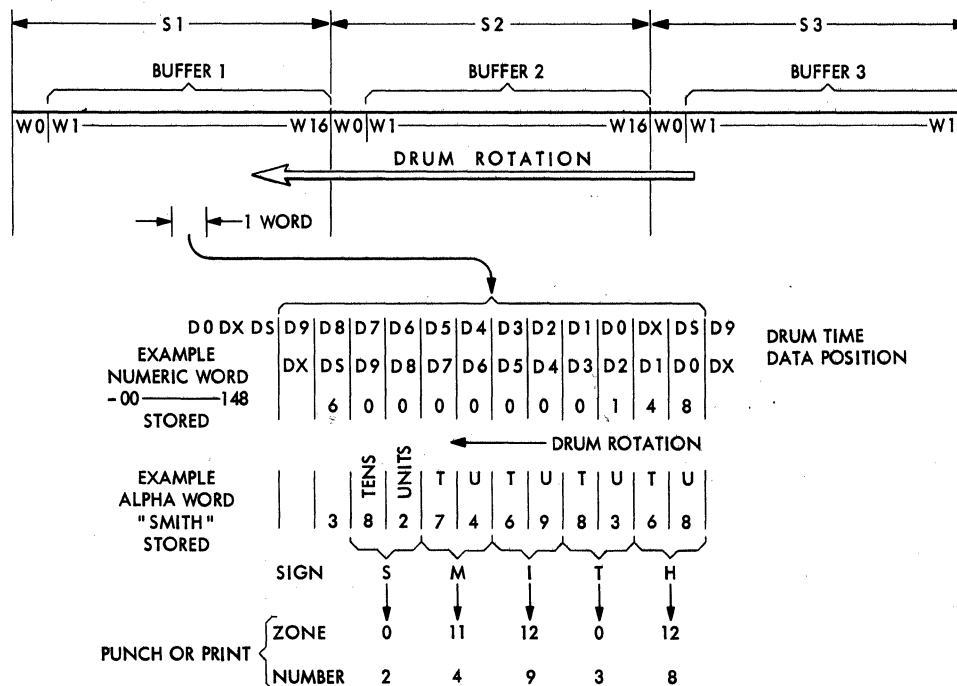


FIGURE 3.1-1 OUTPUT BUFFER STORAGE

3.1.00 DATA TRANSMISSION

3.1.01 Drum Data Bus

Data from the drum arrives at the translator in a coded 0, 1, 2, 3, 6 form, serial by digit and parallel by bit. Each buffer is read, in turn, as the drum revolves, and the drum output is not gated prior to entering the translator. Information comes from the drum as indicated in Figure 3.1-1. Note that the normal A&P and core-storage designations for digit position are reversed on the drum; D0 position becomes

Alpha Delay. The numeric representation of the zone and numeric portions of each alphabetic character must be analyzed by the translator at the same time to be entered into the correct punch or printing position (output relay). The zone representation, (6, 7, or 8) is available from the drum at odd digit time (D7, D5, D3, D1, DX). Each of these impulses must be delayed until the next following even-digit time so that the numeric and zone impulses for each character can be analyzed and routed (later in the circuitry) to the same output relay.

The delay latch (Figure 3.1-3) accomplishes this delay. It is turned on by switching the drum bus lines with odd-digit and Alpha Wd. Pulses. The delay latch remains on during the following digit time and is turned off at A + B time of the next odd digit. Thus, the tens-position zone bits are available for analysis with the units position numeric bits at even-digit time.

3.1.03 Circuit Breaker Translate

The output buffer is scanned as follows to determine which of the 80 output relays must be picked:

1. At all 12 cycle points and control time for the punch.
2. At all 12 cycle points, control time and sign time for the printer.

The 12 translate CB's each make for one cycle point 9 through 12. While the output machine is in a position to translate a specific digit, the corresponding translate CB is made. For example, approximately a cycle point ahead of 8 punch time, the 8 translate CB makes, and only the translator outputs representing 8's pass through the CB translator. Because only one of the 12 CB translators is used at a time, they are OR'ed together and then gated with the down condition of the tens-ring output.

3.1.04 Buffer Scan Rings

By use of a ring matrix, the outputs of an 8-position ring are switched with the outputs of a 10-position ring to provide the same sequence of test gates that an eighty-position ring provides (Figure 3.1-3). The usual 80-position matrix ring consists of a tens-position ring for the units drive and eight position ring for the tens drive. However, because of the demands on the circuit during control-information time, the 7603 uses a 10-position ring for tens drive and an eight-position ring for units drive.

Both rings are reset to zero at D9-D8 of W1, just prior to scan time. With both rings at zero, data arrives from the translator. A Sample Buf 1, C + D pulse, samples the output of the ring matrix and causes the pick of output relay 1 which in turn feeds Storage Exit hub 1. The next following controlled-ring drive BP advances the units ring to its 1 position. A Sample Buf 1, C + D pulse samples the data line and causes the pick of output relay 2 if data is present. The units ring continues to advance to 7, gates on the tens ring 1 and resets to zero. The next position sampled is 9. The operation continues until the rings advance to 97, if the control panel is wired correctly. A ring is made after scanning the entire buffer and the ring is reset prior to the next operation. The table in Figure 3.1-3 shows the output relay picked for each tens and units ring setting.

CI =

all emitter latches
forced on at CI time
except 11, 12 (no emitter latches
on for sign time)

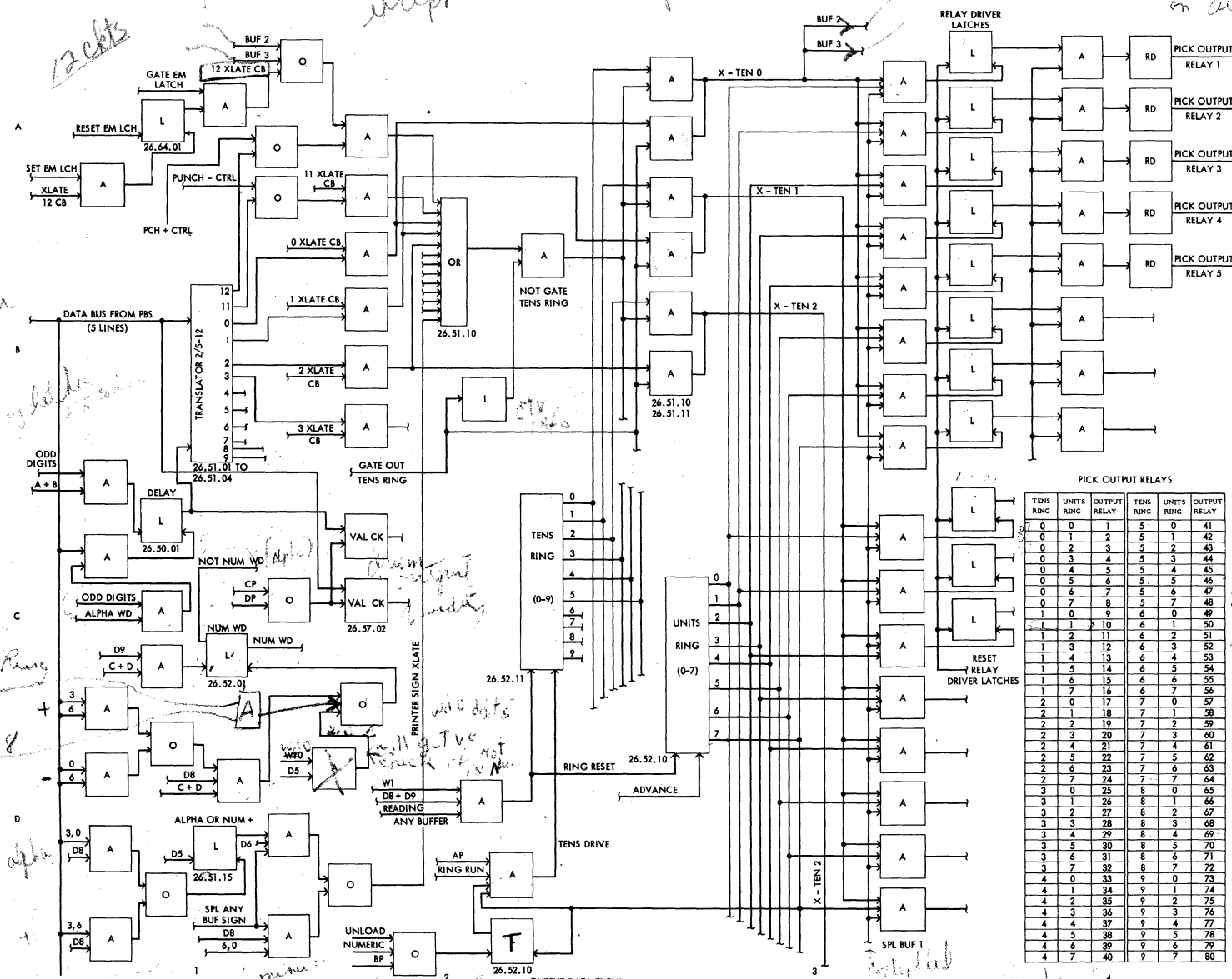
on numeric wds
every relay should pick
at least once - except
on alpha blanks

1 relay could pick
a word of 5 times

from drum

56 y bits

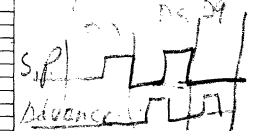
gate out
w/ dig 8



PICK OUTPUT RELAYS

TENS RING	UNITS RING	OUTPUT RELAY	TENS RING	UNITS RING	OUTPUT RELAY
0	0	1	5	0	41
0	1	2	5	1	42
0	2	3	5	2	43
0	3	4	5	3	44
0	4	5	5	4	45
0	5	6	5	5	46
0	6	7	5	6	47
0	7	8	5	7	48
1	0	9	6	0	49
1	1	10	6	1	50
1	2	11	6	2	51
1	3	12	6	3	52
1	4	13	6	4	53
1	5	14	6	5	54
1	6	15	6	6	55
1	7	16	6	7	56
2	0	17	7	0	57
2	1	18	7	1	58
2	2	19	7	2	59
2	3	20	7	3	60
2	4	21	7	4	61
2	5	22	7	5	62
2	6	23	7	6	63
2	7	24	7	7	64
3	0	25	8	0	65
3	1	26	8	1	66
3	2	27	8	2	67
3	3	28	8	3	68
3	4	29	8	4	69
3	5	30	8	5	70
3	6	31	8	6	71
3	7	32	8	7	72
4	0	33	9	0	73
4	1	34	9	1	74
4	2	35	9	2	75
4	3	36	9	3	76
4	4	37	9	4	77
4	5	38	9	5	78
4	6	39	9	6	79
4	7	40	9	7	80

Sample pulses
last. then some
pulses



Stop with units
Ring ready for next
wd.
(except CI time)

FIGURE 3.1-3 OUTPUT DATA FLOW

Part
trigger next
light ring
cannot on at Ap with units plus 7

Sample also
100%

Use any units from
CI time

3.1.05 Relay Driver Latches

The 80 outputs of the scan matrix feed 80 relay driver latches which act as a row buffer for the 1 cycle point storage of each row of punches (or print).

3.1.06 Relay Drivers

The output of the relay driver latches is gated before the beginning of each cycle point to operate selected relay drivers which, in turn, cause punching of the selected columns.

3.2.00 OUTPUT SCAN MATRIX CONTROL

3.2.01 Introduction

The word-size control circuits (Figure 3.2-1) provide a flexible method for punching or printing the contents of output buffer storage by control of the scan matrix.

The 160 numeric digit capacity output buffer may be punched or printed in any of the following combinations:

1. Any combination of alpha and numeric digits up to a total of 80 characters.
2. Any combination of word lengths (1-10 digits) if the total digits do not exceed 80, and the total number of words do not exceed 16.
3. Any number of numeric word signs up to 16.

Example: To illustrate the operation of the output scan matrix control, a specific example is used to show the major operations involved in the output of various size alpha and numeric words. In the discussions which follow, the punch control panel wiring is as shown in Figure 3.2-2.

Wiring of word exits to punch causes the matrix scan rings to advance in such a way as to scan out only the number of digits wired. The rings must be run out to 80 by proper wiring of the control panel. Because 21 positions are punched ($80 - 21 = 59$), additional positions of ring must be advanced. This is accomplished by wiring the word exit for W6 to Word Size 9, and words 7-11 to Word Size 10 for a total of 59 (Figure 2.3-2). Even though the buffer might be loaded, nothing is punched for these words because no storage exit control panel wiring is in place.

3.2.02 Scan Matrix Control Units (Figure 3.2-1)

Word Exit Control

Each of the 16 word-exit hubs is tested in turn as the drum revolves through the 16 words of Output Buffer 1. The test impulse is an early-word gate which occurs one word early for each word exit. For example, the test impulse furnished the word 2 exit hub occurs during drum W1 time.

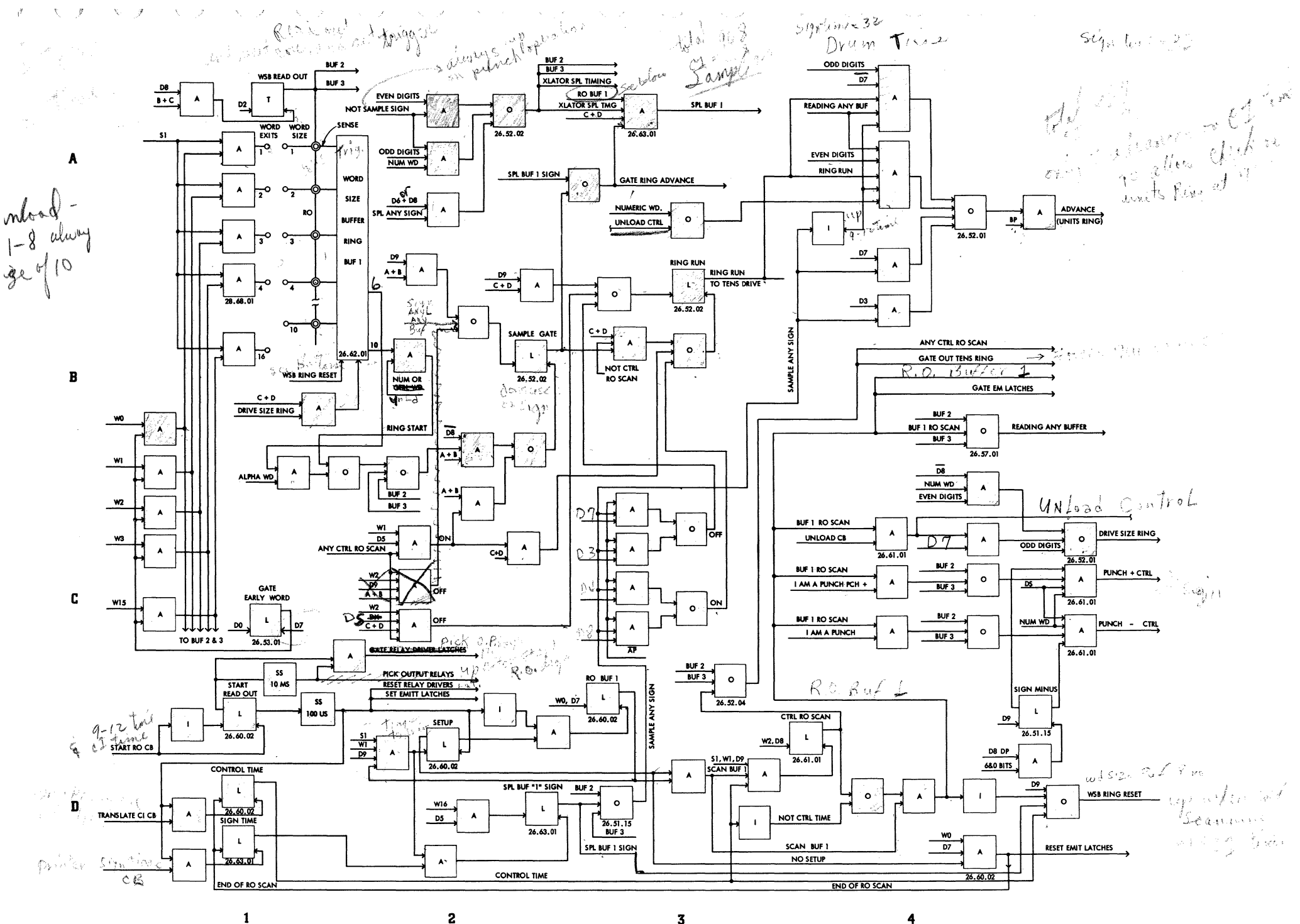


FIGURE 3.2-1 OUTPUT BUFFER DATA FLOW CONTROLS

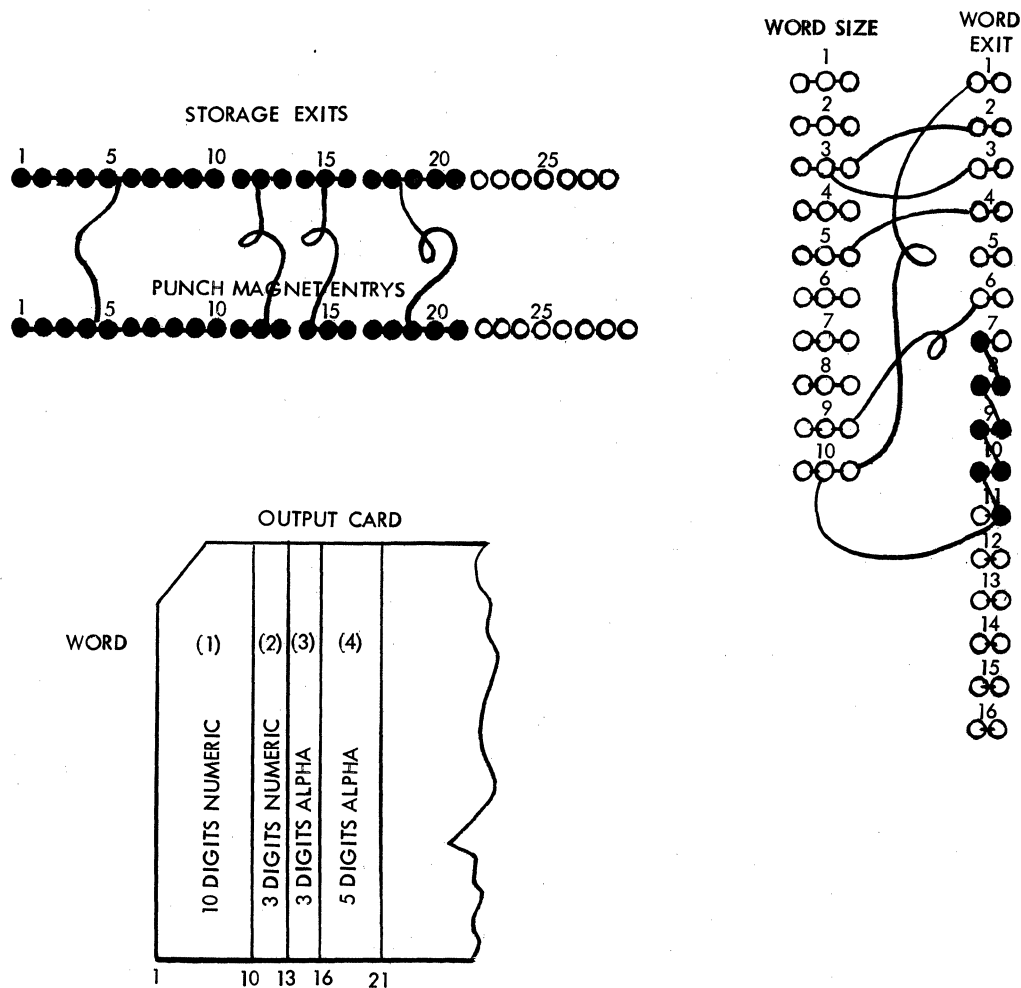


FIGURE 3.2-2 PUNCH WIRING AND CARD FORMAT

Word Size Control

The 10 word-size hubs accept the early-word gates through the control panel wiring and cause the word-size buffer (WSB) core to set and indicate to the matrix control circuits the size of the word to be punched.

Word Size Buffer Ring

This ring is started during each buffer word time (if control panel wiring is present) by the read out of the WSB core. The ring is advanced each drum digit time except D8 (sign time) on a numeric operation by a controlled C + D pulse. The ring causes the automatic skipping of the scan of the high-order digits of a word of fewer than 10 digits. The ring 6 output is tested on an alpha operation, and the 10 ring output is tested on a numeric operation. The sample gate is turned on by the results of this test.

Sample Gate

The output of this latch controls the ring-run and sample buffer circuits under the following circumstances:

- a. Numeric read-out
- b. Alpha read-out
- c. Control information read-out

Ring Run

The ring-run latch controls the advance of the units and tens output scan matrix drive rings under the following circumstances:

- a. Alpha and numeric operations
- b. Control information operations
- c. Read-out of buffer 1 sign for control purposes (printer only)

3.2.03 Scan Matrix Control Circuits (Figures 3.2-1, 3.2-2)

Read-Out of 10 Numeric Digits

Sensing the Numeric Word. Either a + or - sign sensed at D8 C + D time will turn on the numeric-word latch for the duration of the word (Figure 3.1-3, Section 1C).

Setting the Word-Size Core. The early-word gate for word 1 (during W0 time) is control-panel wired to set the 10 WSB core. This core remains set on until it is read out by the D8, B + C to D2 time RO gate during W1.

Sample Gate. The word-size 10 trigger output is sampled by the next A + B pulse after D8 (sign) time to turn on the sample gate. The sample gate switches with both odd and even digits on a numeric word to furnish 10 Sample Buffer 1 pulses which are fed to the output scan matrix to sample the first 10 digits of the drum buffer output. This causes the pick of output relays for columns 1 to 10.

Ring Run. During word-1 time the sample gate switches with a C + D pulse to turn on the ring-run latch. Ring-run output switches with controlled even and odd-digit pulses on numeric word output to generate a series of 10 B pulses which cause the advance of the 8 position units ring from 0 through 7 to 2. When the units ring reaches 7, the ring-output switches with ring-run and an AP to cause the advance of the tens ring from 0 to 1 (Figure 3.1-3). Thus, at the end of the read-out of the ten digits of word 1, the tens ring is at 1 and the units ring at 2, ready to read into output relay 11.

Read Out of 3 Numeric Digits - Word 2

The operation of the scan matrix control circuits on the read out of 3 digits is similar to that for 10 digits. The 3 word size buffer core is set by an early-word 3 pulse. This core is read out by the D8, B + C through D2 time gate during word 2 to cause the start of the word size buffer ring at trigger 3. The ring is advanced at each C + D time by the drive size ring gates until the ring reaches its 10th position. The sample gate and ring run are turned on in the same manner as with the read in of 10 numeric digits. Because both these latches are on for 3 digit times instead of 10, three digits of numeric information are entered in output relays 11, 12 and 13. The tens ring is left at 1 and the units ring at 5. Thus, the next output relay to be picked (if the corresponding digit is to be punched) will be 14.

Read Out of 3 Alpha Characters - W3

Alpha characters are stored on the drum using a two numeric-digit code. Thus, five alpha characters are stored in each ten-digit word on the drum. As discussed previously, the odd-digit positions of an alpha word are delayed for one digit time before entering the translator. Thus, only the even-digit time scan matrix output need be sampled when alphabetic characters are being punched. Control-panel wiring operates in the same manner as for numeric punching, causing the setting of word size core 3. This core is read out in the usual manner to turn on word size trigger 3. On alpha operation the size ring is driven by odd-digit C + D pulses only. Because the maximum size alpha word is 5 digits, the early portion of the 6 trigger output is sampled by alpha word and an A + B pulse to turn on sample gate and, in turn, ring-run. Sample gate is switched with even digit C + D pulses to sample only the even-digit matrix output. Ring-run is switched with odd digits, and with B pulses to advance the ring to its next digit position.

Read Out of 5 Alpha Characters - W4

The operation here is the same as W3 except that the control-panel wiring causes the word size buffer 5 core to be set. The trigger ring is advanced in the same way as with word 3. The sample gate and ring run are on for a longer time, allowing the scanning of five alpha digits.

Read Out of W5-W16

Because word 5 exit is not wired on the control panel, the WSB core is not set, no sampling takes place, and the rings are not advanced during W5.

Words 6 through 11 operate in the same manner as words 1 and 2. Words 12-16 are the same as word 5.

3.3.00 PUNCH SIGN OVER UNITS OPERATION

3.3.01 Introduction

Minus signs must always be punched under control of the I am a Punch line (Figure 3.2-1). This line is up whenever a punch is connected to Buffer 1. Plus signs may be punched at the option of the programmer under control of the P + control panel hub and the I am a Punch + line.

The sign of a numeric word is available on the drum data bus at D8 drum time. If this sign is to be punched over the units position of the output word, the sign translator output must be fed to the scan matrix at the same drum time as the units position (different punch time, however). Because the units position is scanned at DS drum time (recall that units is in the D0 data position), the sign must also be scanned at DS time.

3.3.02 Data Flow for the Punch Sign Over Units Operation

If W1 is a ten-digit word to be punched in card columns 1-10 and it is desired to punch a minus sign over the units position, the following data flow path elements are used:

1. Punch-Control on at W2 DS drum time
2. 11 X LATE CB made
3. Gate tens ring on
4. Tens ring 1 output on
5. X-Ten 1 line up
6. Units ring 1 output on
7. Relay Driver 10 on
8. Output relay 10
9. Punch Magnet 10

3.3.03 Circuits for the Punch Sign over Units Operation

The circuits used to generate Punch - Control are shown in Figure 3.2-1 and are described by the operation chart (Figure 3.3-1). Note that plus signs (+) are punched only if Punch + is wired on the control panel and if the sign-minus latch is off. The operation is the same as with a minus sign except that it occurs when the 12 X Late CB is made.

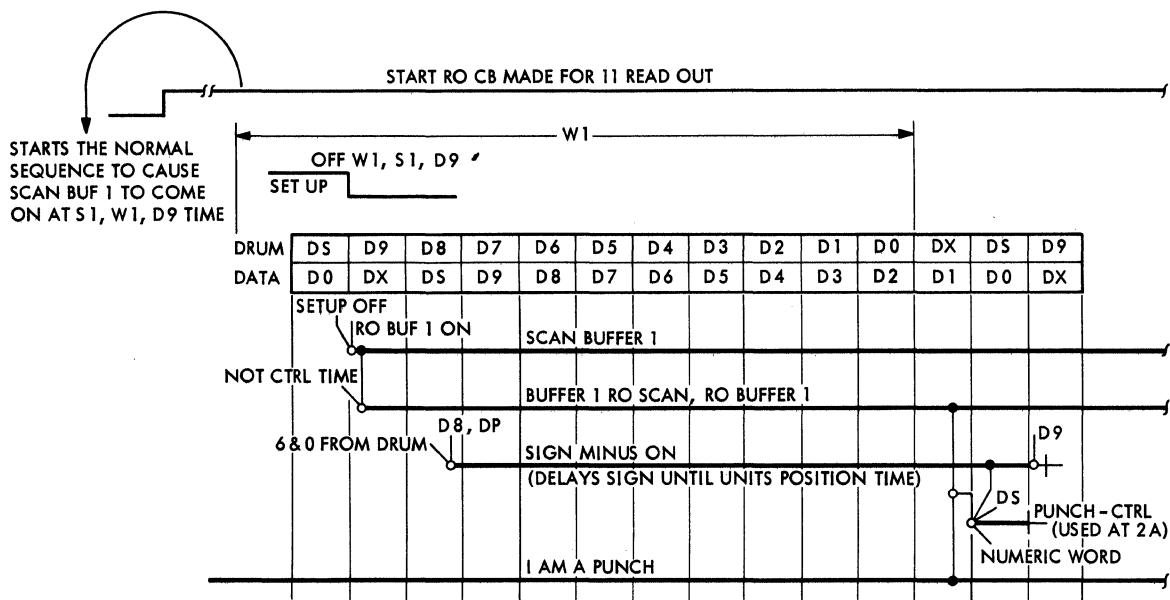


FIGURE 3.3-1 PUNCH SIGN OVER UNITS OPERATION

3.4.00 CONTROL INFORMATION OPERATION

3.4.01 Introduction

At the discretion of the programmer, digits 0 through 7 of word 1 of output may be used for control purposes. The value stored in any of these digit positions is available just before 9-punch or printer time to operate selectors for the control of the information to be punched. Figure 3.4-1 shows the control panel output hubs for control information. For example, if the programmer stored a 3 in output word 1 in the D2 position, output relay 27 would operate, and the control panel hub in the position marked * would emit a control-information impulse. Thus, for any one card to be punched (or line to be printed) one hub in each vertical column would emit an impulse.

3.4.02 Data Flow

Assume that a 1 is stored in the D1 position of word 1. Data flow to the D1, value 1 control-information hub would be as follows (Figure 3.1-3):

1. Drum data bus
2. Translator, out on 1 line. All emitter latches are forced on at C.I. time so the 1 X LATE CB line is up.

		DIGIT POSITION OF WORD 1							
		7	6	5	4	3	2	1	0
		0	1	2	3	4	5	6	7
DIGIT VALUE STORED IN WORD 1	0	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)
	1	(9)	10	11	12	13	14	15	16
	2	(17)	18	19	20	21	22	23	24
	3	(25)	26	27	28	29	30	31	32
	4	(33)							40
	5	(41)							48
	6	(49)							56
	7	(57)							64
	8	(65)							72
	9	(73)	74	75	76	77	78	79	80

CHART SHOWS THE POSITION OF CONTROL PANEL HUBS AND THE NUMBER OF THE OUTPUT RELAY OPERATED FOR EACH CI OUTPUT.

FIGURE 3.4-1 CONTROL INFORMATION

3. X-ten 1 line via switch controlled by Gate Out Tens Ring switching.
4. Sample Buffer 1, Units Ring 1, X-Ten 1, AND switch.
5. Relay driver latch 10 and output relay number 10.
6. Punch-Calculator connector PC 10 and CI exit D1, value 1 (Figure 3.4-1) (See Printer WD, Sec 18A or Punch WD, Sec 12A).

3.4.03 Control Information Circuit Operation

Objectives:

1. Make C.I. pulses available on the control panel prior to 9 time only.
2. Time the Buffer 1 section of the drum (S1) to the C.I. CB pulse.
3. Scan only W1, Digits 0-7, out of the buffer 1 drum section.
 - a. Sample Buffer 1, D0-D7
 - b. Advance the digit ring 0-7
 - c. Prevent the tens ring from operating

Control Information Pulse

As shown on the timing charts for punch and printer operation (Figures 3.6-2 and 4.0-1), the control time CB makes 4 cycle points before 9 time and just before the Start Read Out CB, for control information time. Section 19A of the punch wiring diagram shows how the C.I. exits are controlled from 327 1/2 to 350 1/2 degrees only by use of the C.I. time relays. See WD Sections 11-18 for use of the C.I. time points.

Time Drum Sector to C.I. CB Pulse

Reference should be made to the operation chart for control information

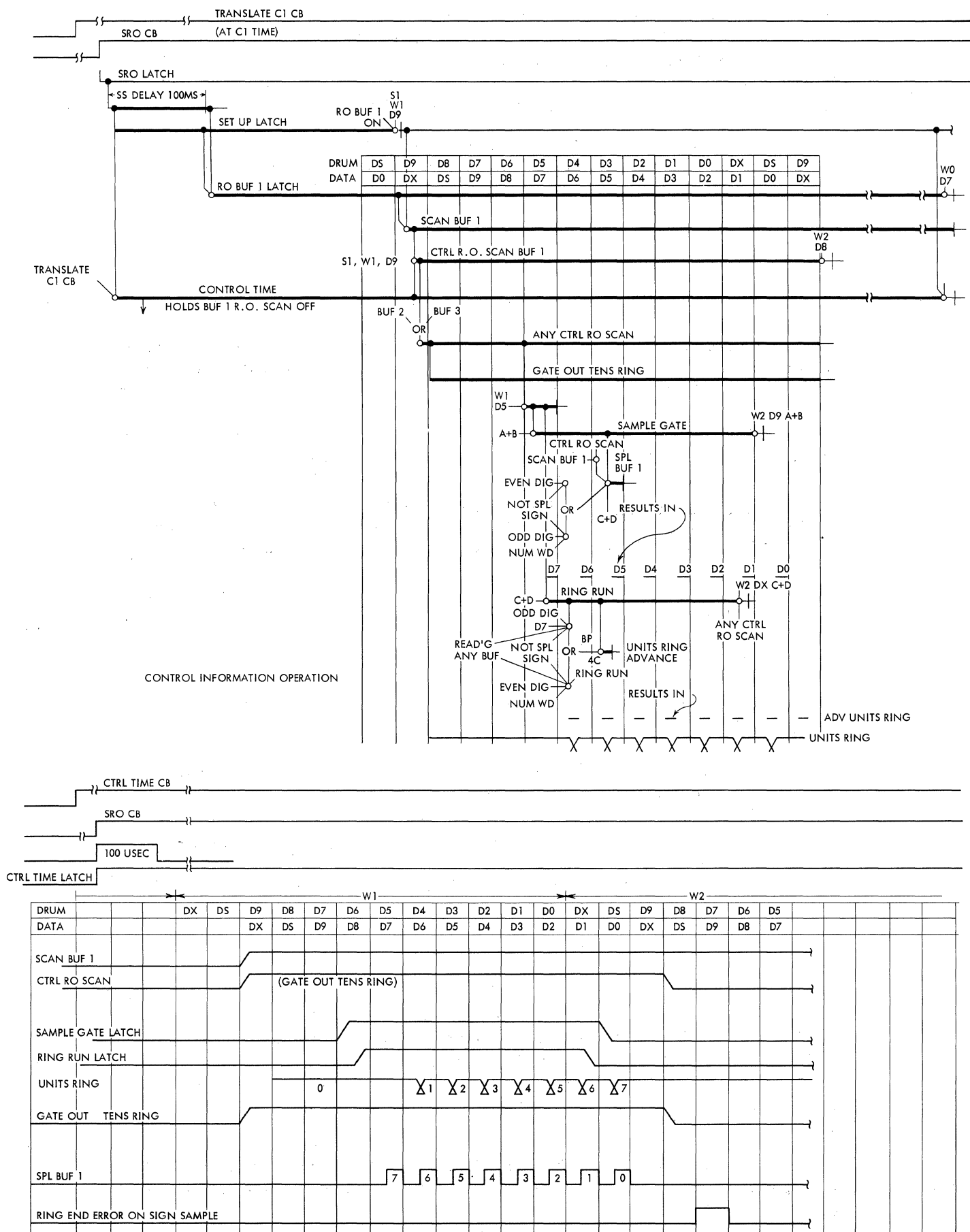


FIGURE 3.4-2 OUTPUT TIMING CONTROL TIME

(Figure 3.4-2), during the following explanation. The normal sequence of events occurs when the Start Read Out (SRO) CB makes. As shown on Figure 3.4-2, this sequence includes the SRO latch, the 100 usec delay, the set-up latch, the RO buffer 1 latch and the Scan Buffer 1 latch. Note that the Scan Buffer 1 latch times the beginning of Buffer 1 to the make of the Start RO CB. Recall that the Scan Buffer 1 latch normally times the read-out of each digit to the drum buffer (review Section 3.6.02).

Because the control time CB is now made, the control-time latch comes on at the same time as the setup latch. The output of the control-time latch switches with Scan Buffer 1 at S1, W1, D9 time to turn on the Control Read-Out Scan Buffer 1 latch.

Scan Word 1

The Control Read-Out Scan Buffer 1 latch controls the following:

Sample Gate. This latch output switches as shown on the operation chart to provide C + D pulses to sample the scan matrix output at D5 through DS (storage word digit positions) time of Buffer 1, Word 1 only, thus sampling the D7-D0 data.

Ring Run. This latch output provides the switching necessary to cause the seven advance units ring B pulses which move the units ring from 0 to 7.

Gate Out Tens Ring. This gate prevents the normal translator output from reaching the units matrix switching via the tens switching and sets up a direct path from the translator output to the units scan matrix switching (Figure 3.1-3).

3.5.00 UNLOAD

3.5.01 Introduction

Words 1-8 of the output buffer area are punched or printed as a result of impulsing the unload hub at control information time.

1. Any of the eight unload words which are numeric will be punched or printed as ten digit (and sign) numeric words.
2. Any of the eight words (except the first) which is alphanumeric will be punched or printed as a 5-character word if the appropriate unload alphabet word hub is impulsed at control information time.
3. Word 1 is reserved for control information and may not be unloaded as an alpha word.

3.5.02 Unload Circuits

1. The IBM 7400 Printer wiring diagram (Section 36A) shows how a C.I. pulse picks R75, Unload. R75 holds along with the remainder of the unload relays in Section 36. The R78-5 through 12 n/o points (Section 37B) connects early word gates (PC 155-162) for words 1-8 to the Word Size Entry 10 hub. This is connected via PC 180 to the 10 WSB core (Figure 3.2-1). Thus, each output word is unloaded as a ten-digit word.

2. Similarly, the IBM 7550 diagram (Section 25B) shows how the early-word gates for W1 to W8 are routed to the Word Size Entry 10 hub to set the 10 WSB core.

3. The unload signal is developed in the output machine at C.I. time and is sent to the input/output synchronizer. Section 36A of the printer wiring diagram shows how the C.I. pulse is brought through the unload hubs to PC 108. Figure 3.2-1 shows how the unload CB signal from punch or printer switches with Buf 1 RO Scan to cause an unload-control signal.

4. The unload-control signal is used in Figure 3.2-1 to advance the units ring each digit time whether the output word being unloaded is numeric or alpha. Figure 3.2-1 also shows that the Spl Buf 1 pulses occur only at even-digit time with alpha words. Because the units ring advances each digit time, but sampling occurs only at even digit times, only even-numbered output relays can be picked when unloading alpha words.

5. Recall that the odd digits of an alpha word are delayed by the delay latch (Figure 3.1-3) so that they can be analyzed later with the even digits. As just noted in 4, only the even digits are sampled and only even-numbered output relays are picked.

6. The punch wiring diagram (Section 13A and 14A) or printer diagram (Section 19-22) show how the even-numbered output relay PC connector outputs are switched so the 5 digit alpha words can be compressed for printing or punching like this, ABCDE, rather than A B C D E. Note that in the case of either punch or printer, the unload alpha hubs (Printer, Sec 35B) must be impulsed by a C.I. pulse to provide for switching into this arrangement.

3.6.00 SYNCHRONIZATION TO THE OUTPUT MACHINE

3.6.01 Introduction

At each cycle point an analysis is made at the translator to determine which digits should be punched or printed at that particular cycle point. The result of this analysis is scanned, sampled, and allowed to pick output relays. This operation is discussed in detail in Sections 3.1.00 and 3.2.00. The process is synchronized to the output machine CB's by the following circuits.

3.6.02 Sync Circuits (Figures 3.6-1 and 3.6-2)

As shown in Figure 3.6-1, the read-out of 9's from the drum buffer begins one cycle point early with the make of the start read-out CB. A 100 usec single-shot delay is set up immediately. This allows time for the reset of relay-driver latches and the setting of the 9 emitter latch before beginning the search for the first word of Buffer 1. The setup latch is also turned on at this time. The delay impulse also prevents more than one turn on of the setup latch for each make of the SRO CB.

At the end of the delay, RO Buffer 1, after a variable length of time, switches with S1, W1, D9 to turn off the setup latch and cause a Scan Buffer 1 signal. This latch remains on for the 16-word duration of the read out of all 9's in the buffer and causes the development of the following additional gates:

1. RO Buffer 1 signal (Section 2D, Figure 3.2-1)
2. Buffer 1 RO Scan (Section 4D, Figure 3.2-1)
3. Reading any buffer (Buffer 1 RO Scan OR'ed from the other buffers, Sec. 4B, Figure 3.2-1).
4. "9" X Late CB. (Turned on each cycle point by switching RO Buffer 1 with the operated emitter latch. The 9 X Late CB gate is created to sample the decoded translator output.)

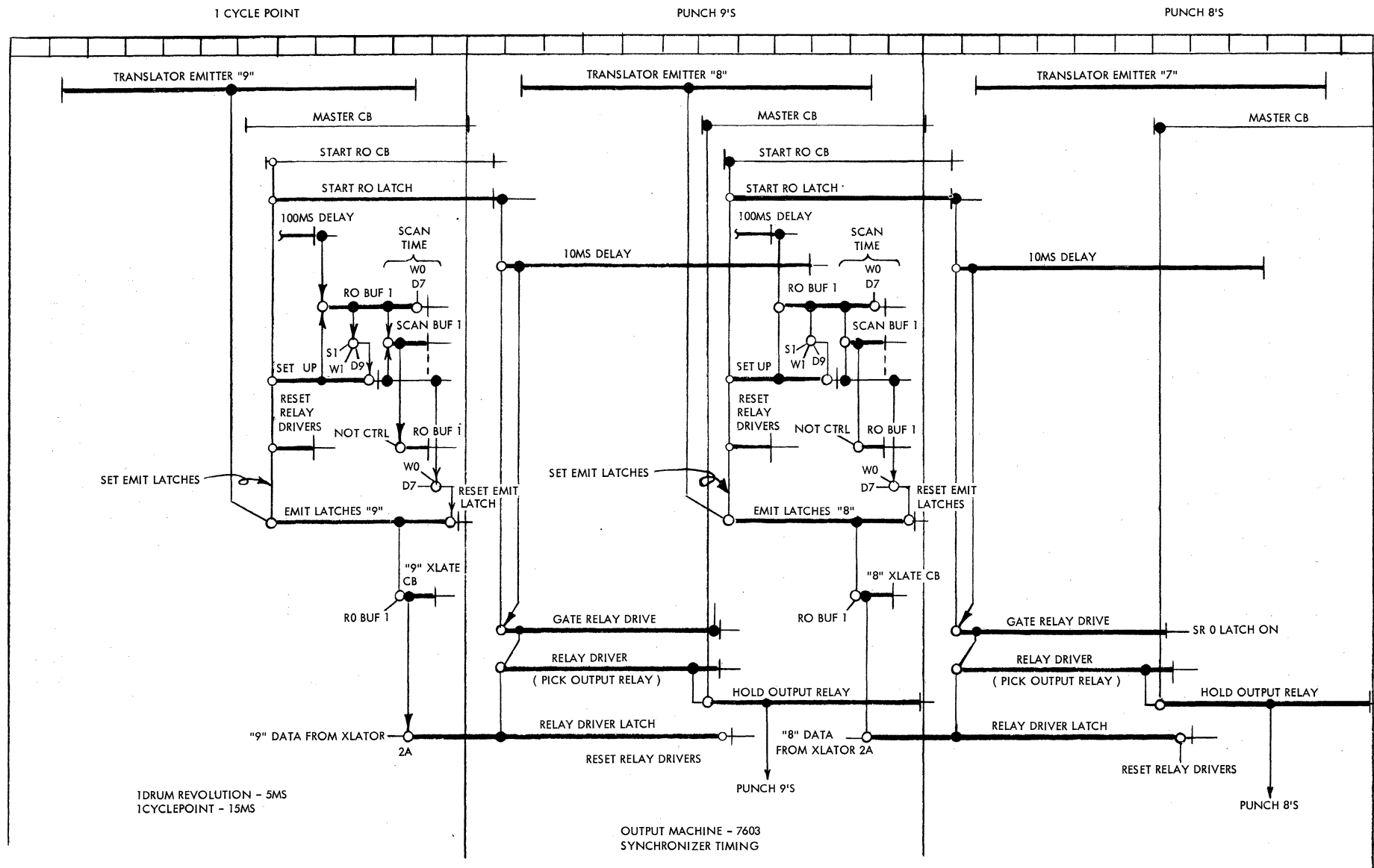


FIGURE 3.6-1 OUTPUT MACHINE - 7603 SYNCHRONIZER TIMING

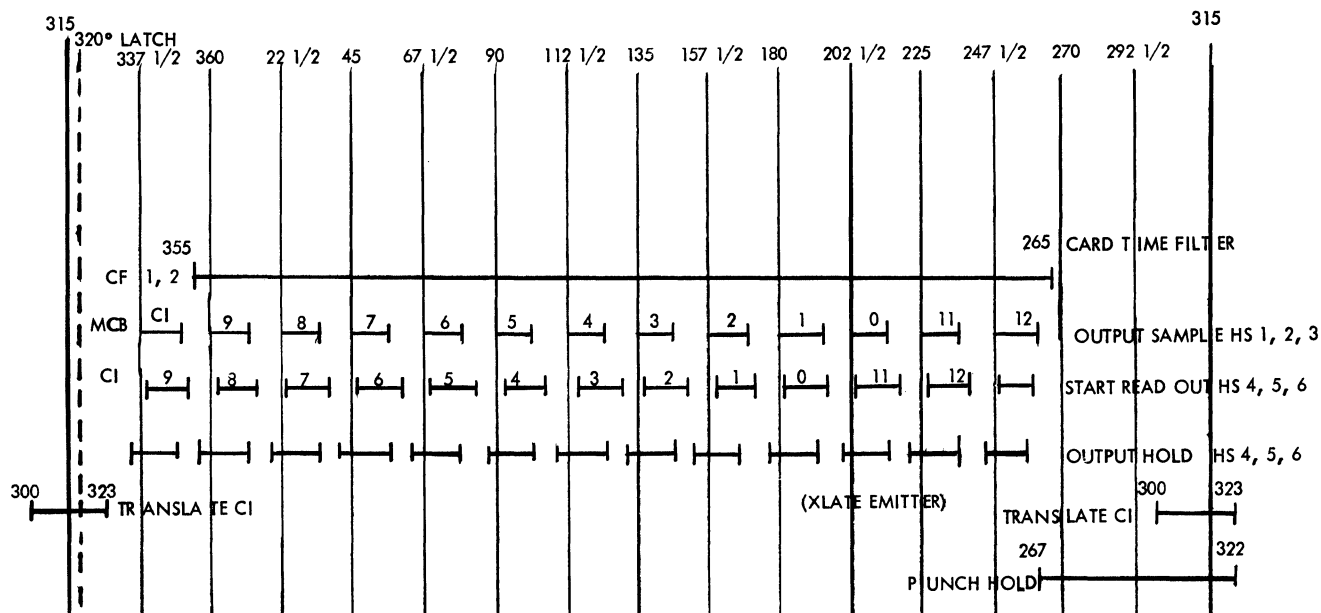


FIGURE 3.6-2 OUTPUT MACHINE TIMING (PUNCH)

The "9" data after passing through the translator and scan matrix operates a relay-driver latch. When the SRO latch goes off a 10 ms delay is started. With the delay single shot on and the SRO latch off, a gate relay driver latch signal is provided to transfer the row buffer (relay-driver latch) contents to the output relays. The output relays hold through the punch master CB's.

The same process is repeated again during 9 cycle point time for the read out of 8's into the relay driver latches and output relays. The main difference between the two operations is the "8" EM latch coming on instead of the "9."

3.7.00 SYNCHRONIZATION TO THE A-P CIRCUITS

Introduction

Figure 3.7-1 shows the circuits required to time the transfer of data from the word-buffer register to the drum, signal the beginning of the punch or printer cycle, and erase the output drum buffer in preparation for the next output operation. Figure 3.7-2 shows an operation chart of the synchronization to the A&P circuits.

Before the write operation code signals arrive at the input/output (IPOP) synchronizer, the following actions have already occurred in the A&P unit:

1. The first word to be transferred to the drum is in the WBR.
2. The record-control word is in the auxiliary register and the first start address of the RCW has been one-upped in preparation for the read-out to the WBR of the second word to be transferred to the drum buffer.
3. The A&P unit program ring has been stopped, and no additional output words can be requested from core storage until the program ring is restarted by the DX Start transfer impulse from the IPOP Synchronizer.

The transfer, punch (or print) and erase operations function as follows (Figures 3.7-1 and 3.7-2).

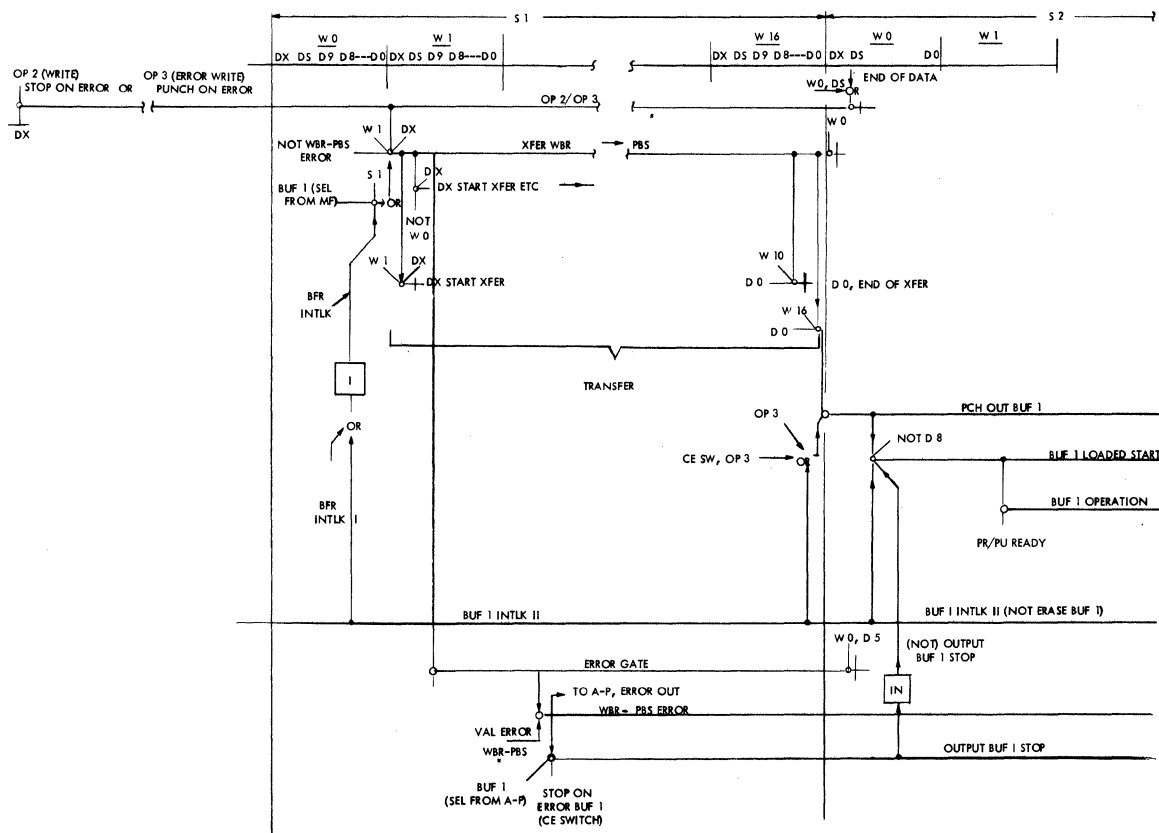


FIGURE 3.7-2A TRANSFER WBR TO PBS, PUNCH AND ERASE SEQUENCE

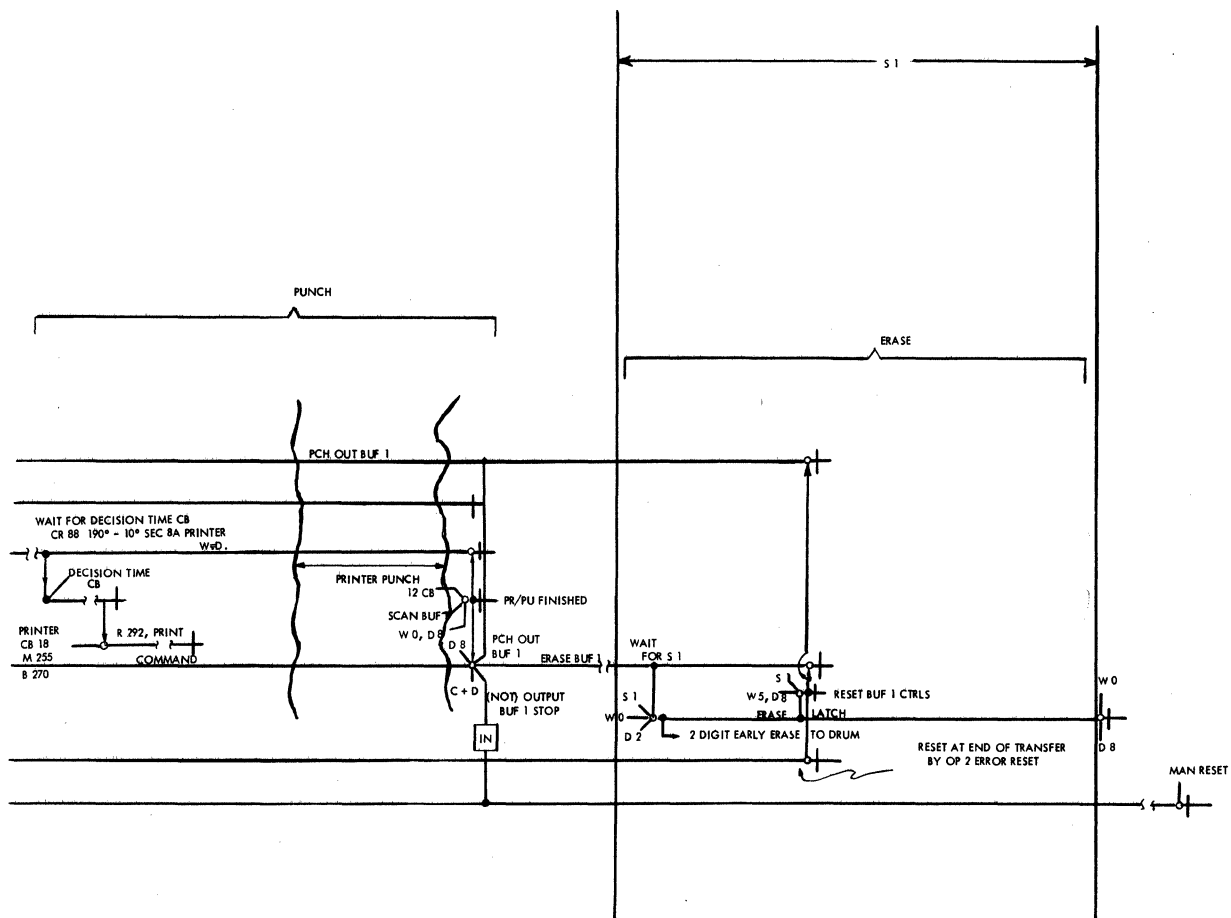


FIGURE 3.7-2B TRANSFER WBR TO PBS, PUNCH AND ERASE SEQUENCE

See new Handout

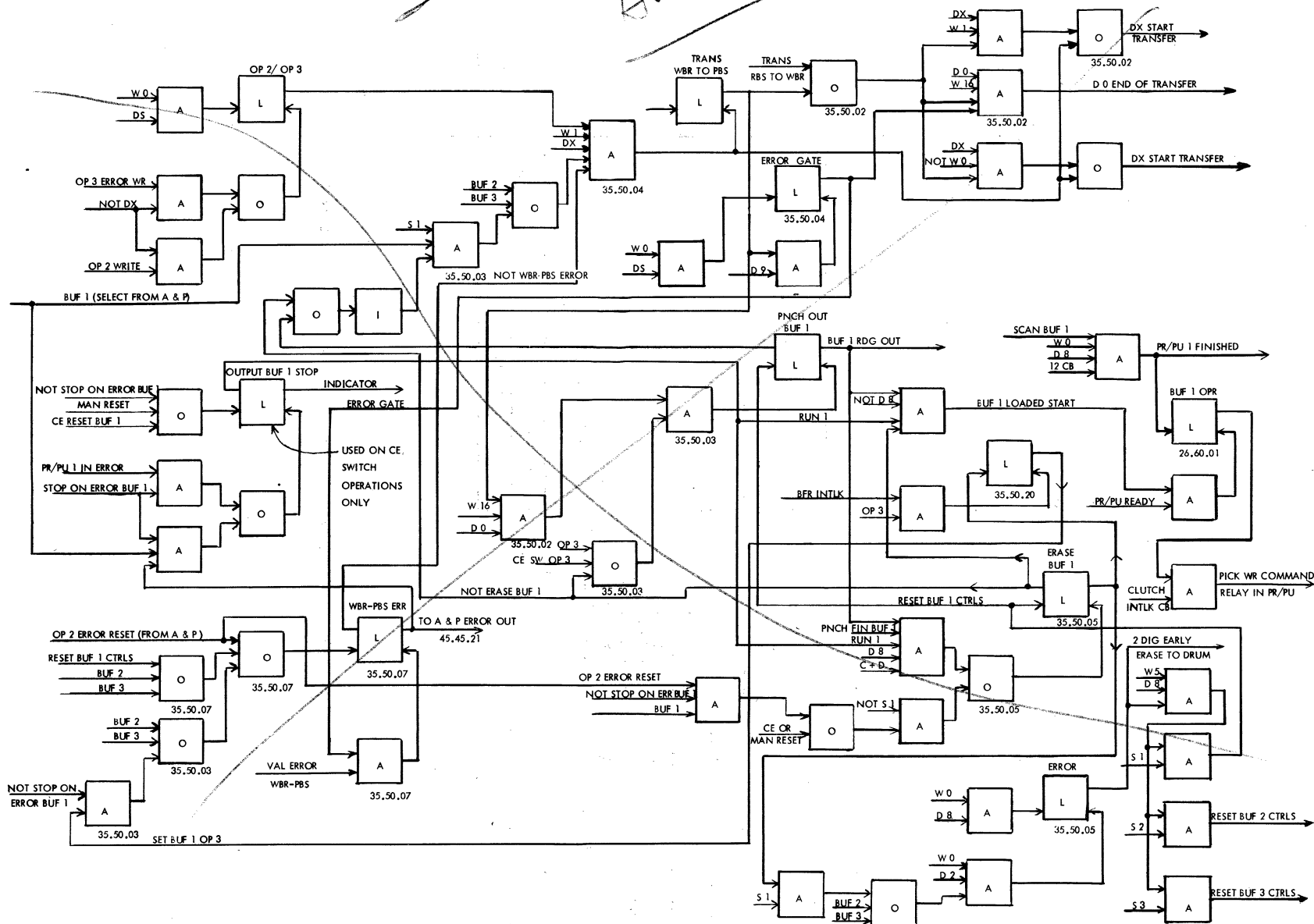
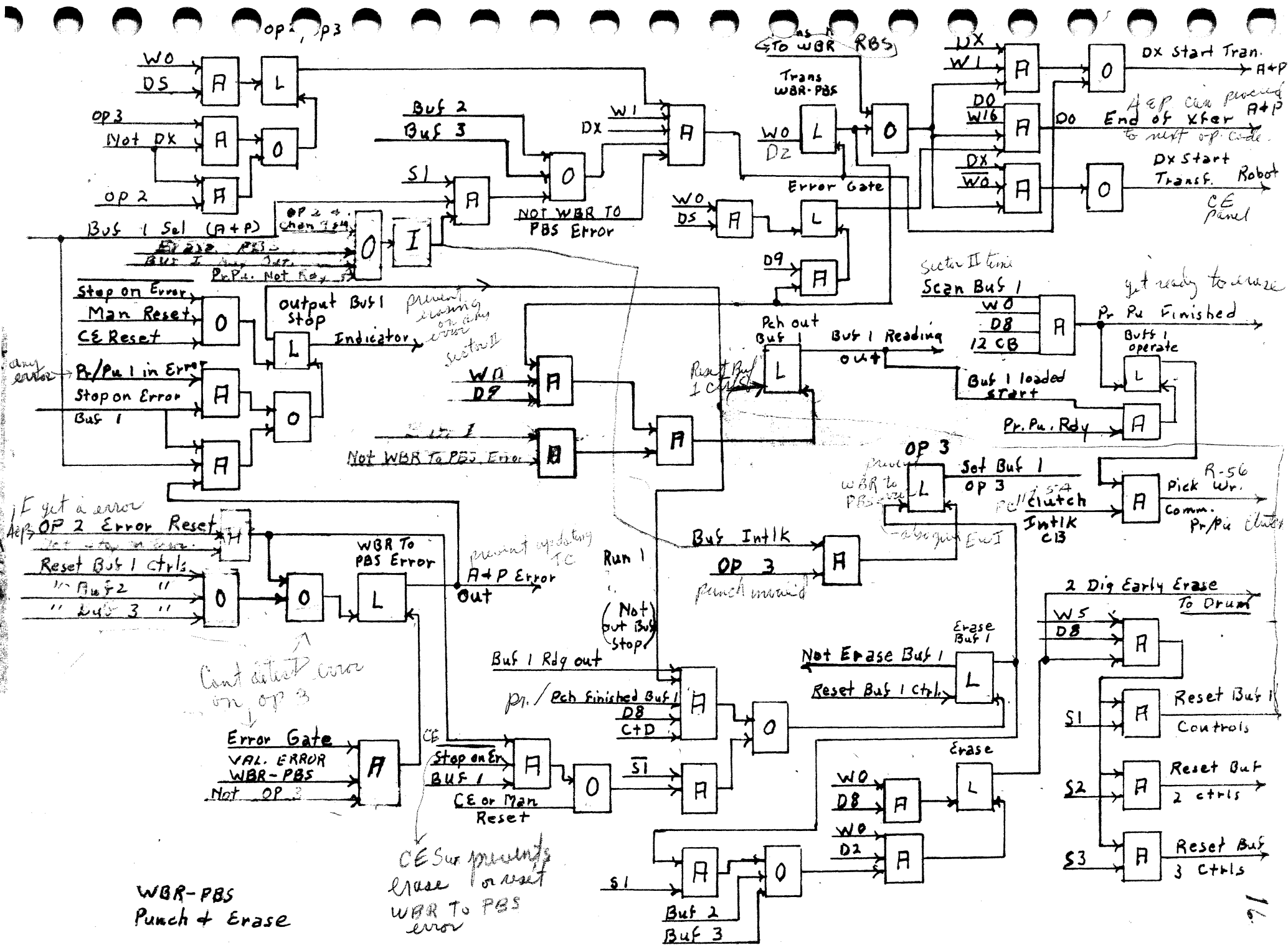


FIGURE 3.7-1 CIRCUITS FOR TRANSFER WBR TO PBS, PUNCH, AND ERASE



Transfer from WBR to PBS

The Op Write and Buffer 1 Select signals switch with Drum, S1, W1, DX gates to turn on a Transfer WBR to PBS latch if the PBS is not already reading out or being erased. The DX Start Transfer signal is returned to the A&P unit at DX of W1 to signal the WBR to begin the serial transfer of data from WBR to drum, under control of record control words.

The end of the data transmission to the PBS is signalled by a W16, D0 signal which is returned to the A&P circuits at the end of the designated output-buffer time. This stops the data transmission, regardless of control by the RCW system. A W16 D0 signal also turns on the Punch Out Buf 1 latch, if the Erase Bfr 1 latch is off (Assume Op 2).

Start the Punch

If the Erase Buffer 1 latch is off and if no CE panel control is on (Output Buf 1 Stop, Off), the Buf 1 Loaded Start signal is brought up. When the punch or printer decision time CB makes and the printer or punch is "ready" (i.e. cards run in on punch), the print (or punch) command relay is picked to start a punch print cycle.

Erase Buffer 1

At the completion of the punching of the 12 holes, a Printer/Punch (PR/PU) finished signal turns on the Erase Buffer 1 latch. The erase latch is turned on during the next Sector 1. This causes the erase of Buffer 1 in preparation for the next transfer from the WBR on the next output operation.

3.8.00 CHECKING CIRCUITS

3.8.01 Output Buffer Validity Check

Figure 3.8-1 shows the positive logic for the validity check circuits. The Val Ck circuit outputs remain positive as long as valid information is being transmitted. Latches 1 and 2 are turned on each CP time and must be turned off each DP time by the Val CK circuit. This checks the validity of the drum data, as well as the operation of the Val Ck circuits.

If Latch 1 is not turned off, the On output switches with an A + B test and the On output of the Latch 3 to turn on the Validity Error Buffer 1 latch. Latch 3 is turned off when data is not being sampled, so no validity check is made unless data is actually being sampled.

Latches 2 and 4 work in a similar manner on an alpha operation only to check the alpha-even digits (units position) which come directly from the drum. The delay-latch output of alpha-odd digits (tens position) at even-digit time is checked by Latch 1 as just described.

Sign does not get into delay latch

- 1 manual Reset holds it reset
- 2 CP 3 code
- 3 decision time
- 4 punch on Buffer output

light thinks if not wrong stop

(gives impulse on control panel)

vs printer/punch (wvi)

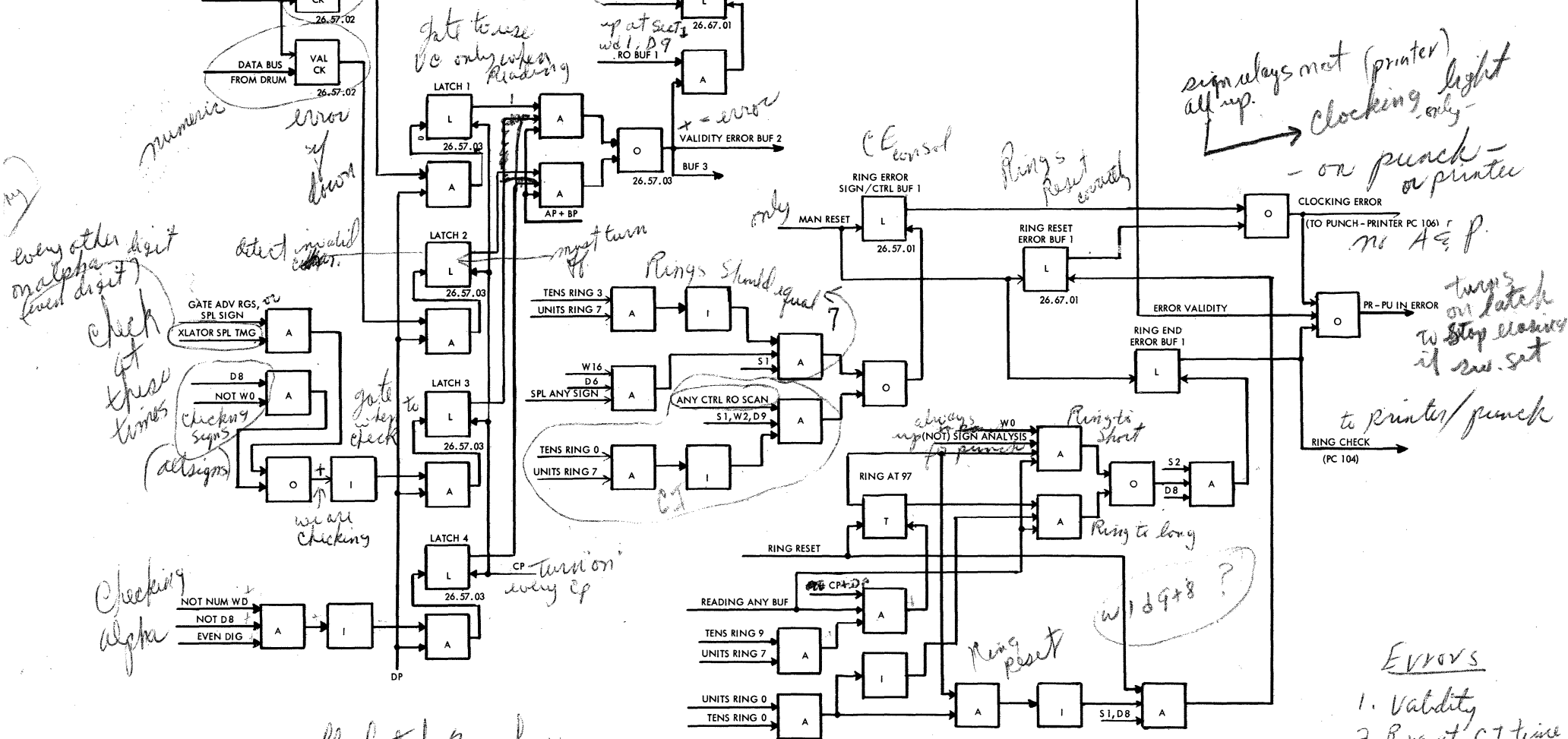


FIGURE 3.8-1 OUTPUT ERROR CIRCUITS

Errors

1. Validity
2. Ring at CI time
3. Ring at 97
4. Ring reset correctly

3.8.02 Scan Matrix Drive Ring Check

Ring Drive at Scan Time Check

The operator must wire the control panel to read out a total of 80 digits from the output buffer. In doing this, he forces the scan drive rings to advance to 97. As shown on Figure 3.8-1, the following checks are made on the ring circuits.

Rings Advanced to 97. The Ring at 97 latch is turned on sometime during the scan operation by switching tens ring 9 and units ring 7 with B + CP, and a Reading Any Buffer signal. If the ring at 97 latch was not turned on, the Off side output would switch with a (not) Sign Analysis Signal at S2, W0, D8 time to turn on the Buffer 1 Ring End Error latch at the end of Buffer 1.

Rings Did Not Advance Beyond 97. An additional drive pulse to both the units and the tens rings after sampling the 80th character drives the rings to 0, 0. No additional drive pulses should occur. This condition is checked by switching Reading Any Buffer with the ring at 97 latch output. If the units and tens ring are not at zero at the end of the buffer (S2, D8), the Ring End Error Buf 1 latch is turned on.

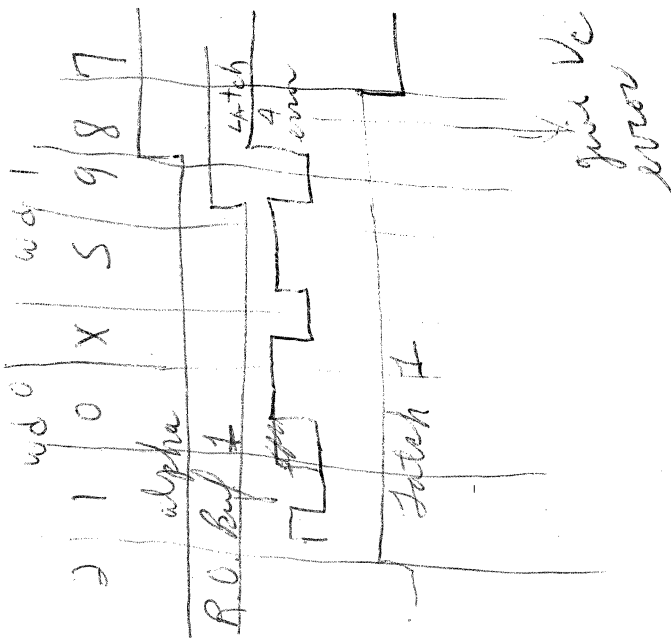
Rings are Reset to Zero. At the beginning of each buffer read-out time (W1, D9 + D8, Reading Any Buffer) the rings are restored to zero. If this has not occurred by S1, D8 of ring-reset time, the Ring-Reset Error Buf 1 latch comes on.

Ring Drive for Sign Sample Check

When the signs of the 16 words of output buffer storage are being sampled for printer control purposes, the rings must drive through 32 positions and end at 37. This condition is checked by switching Spl Any Sign, with (not) ring 37 at S1, W16, D6 time. If the rings are not at 37 by the end of the last sign sample, the Ring Error Sign/Control Buf 1 latch is turned on.

Ring Drive for Control Information Check

The units ring should drive through 8 positions during word one time of Buffer 1. This condition is checked in a manner similar to sign sample check.



4.0.00 PRINTING, CIRCUIT DESCRIPTION

The output buffer circuits operate with the printer in the same manner as with the punch with the following exceptions. Figure 4.0-1 shows the Printer Data RO timing.

4.1.00 PRINTER SIGN READ OUT FOR CONTROL

4.1.01 Introduction

Sixteen sign control exits are provided on the printer control panel for the control of selectors. To operate selectors for the line to be printed, these hubs must be hot prior to 9 time. Because normal sign time comes after 9-0 time, special means must be provided to make the sign information available early. The signs of the sixteen words of punch buffer storage are scanned out into the output relays 1-32 at printer sign time. Output relays are operated as follows:

	W1 - sign	W1 + sign	W2 - sign	W2 + sign	W3 - sign		W16 - sign	W16 + sign
Output Relays	1	2	3	4	5	-----	31	32

The following sequence of events takes place in the printer (Figure 4.1-1):

1. Odd number (-) output relays cause the pick and hold until after 11 print time of minus relays in the printer (Printer WD Sec 27A (W16) and Sec 36).
2. The printer causes the hold of the output relays in the synchronizer to extend from the usual one to two cycle points (Printer WD Sec 38A, CR 105).
3. On the cycle point just before control information time, a test impulse from the printer checks the printer minus relay for each word against the synchronizer even (+) output relay to be sure that one, and only one, is operated for each word. See Figure 4.1-2 for the circuit and Figure 4.1-1 for the sequence of operation.
4. At control-information time, the minus relays in the printer cause the sign control exits to emit CI pulses (See Printer WD Sec 38B).
5. At 11 print time, the minus relays cause the sign exits to emit 11 print pulses. Similarly, the sign exits emit 12 time print impulses if the corresponding minus relay is not operated (See Printer WD Sec 29, 30B).

4.1.02 Printer Sign Read Out Data Flow

The sign-data flow lines from the drum enter Figure 3.1-3 in Sec 1B. The following sequence occurs:

1. The drum data flow lines are sampled for + (6 & 3 bit), - (6 & 0 bit), or alpha (3 & 0 bit) sign at each D8 time (Sec 1D).
2. If the sign is -, a Printer Sign Xlate signal is developed at D8 time and an odd-numbered output relay is operated.

3. If the sign is + or alpha, the Alpha or Numeric + latch is operated to delay the + or alpha indication for later sampling at D6 time.
4. The units ring is advanced at D7 time so the next sample pulse will cause an even (+) output relay to be operated (Figure 3.2-1).
5. If the sign was + or alpha, the Alpha or Numeric + latch output is sampled at D6 time to operate even (+) numbered output relays.
6. The units ring is advanced again at D3 time in preparation for the sign RO of the next word.

4.1.03 Printer Sign Read Out Circuits

The printer sign time CB line is shown on Figure 3.2-1, Sec 1D. The usual Start Read Out, Setup and RO Buffer 1 latch sequence occurs.

When RO Buf 1 comes on, it switches with S1, W1, D9 to signal the beginning of Buffer 1 data. The RO Buf 1, S1, W1, D9 signal then switches with the sign-time latch output to turn on the Sample Buffer 1 Sign Latch. The Sample Buffer 1 Sign latch remains on until the sign of W16 has been sampled. Spl Buf 1 Sign accomplishes the following (Figure 3.2-1):

1. Turns on ring-run for D8 and D4 time so the tens ring can be driven when the units ring goes from 7 to 0 (Sec 3C).
2. Advances the units ring at D7 and D3 time, just after the sampling of minus signs (at D8 time) and plus or alpha signs at D6 time (Sec 3B).
3. Prevents the advance of the units ring under control of ring-run. The Spl Any Sign signal is inverted at 3A to accomplish this.
4. At 2A, Spl Any Sign switches with D6 and D8 to provide Spl Buf 1 pulses which switch with the translator output and units drive ring outputs to turn on the Relay Driver latches.
5. Spl Any Buffer Sign (Figure 3.1-3, Sec 1D) switches with a 6, 0 (- Sign) from the drum data bus at D8 time or with the output of the Alpha or Num + latch at D6 time to provide a printer sign translate signal. This, in turn, switches with not-gate-tens ring and the tens-ring output to provide a X-Ten signal. This, in turn, switches with the units ring outputs to turn on an odd digit, - output relay at D6 time or an even digit + output relay at D8 time. Figure 4.1-3 shows the sequence of operation for both possibilities.

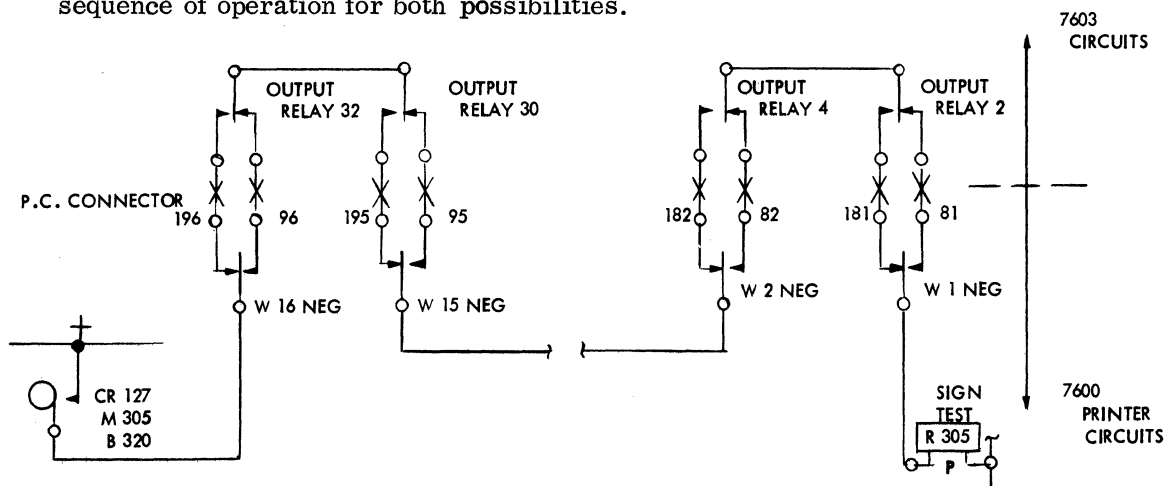


FIGURE 4.1-2 PRINTER - SYNCHRONIZER SIGN TEST CIRCUIT

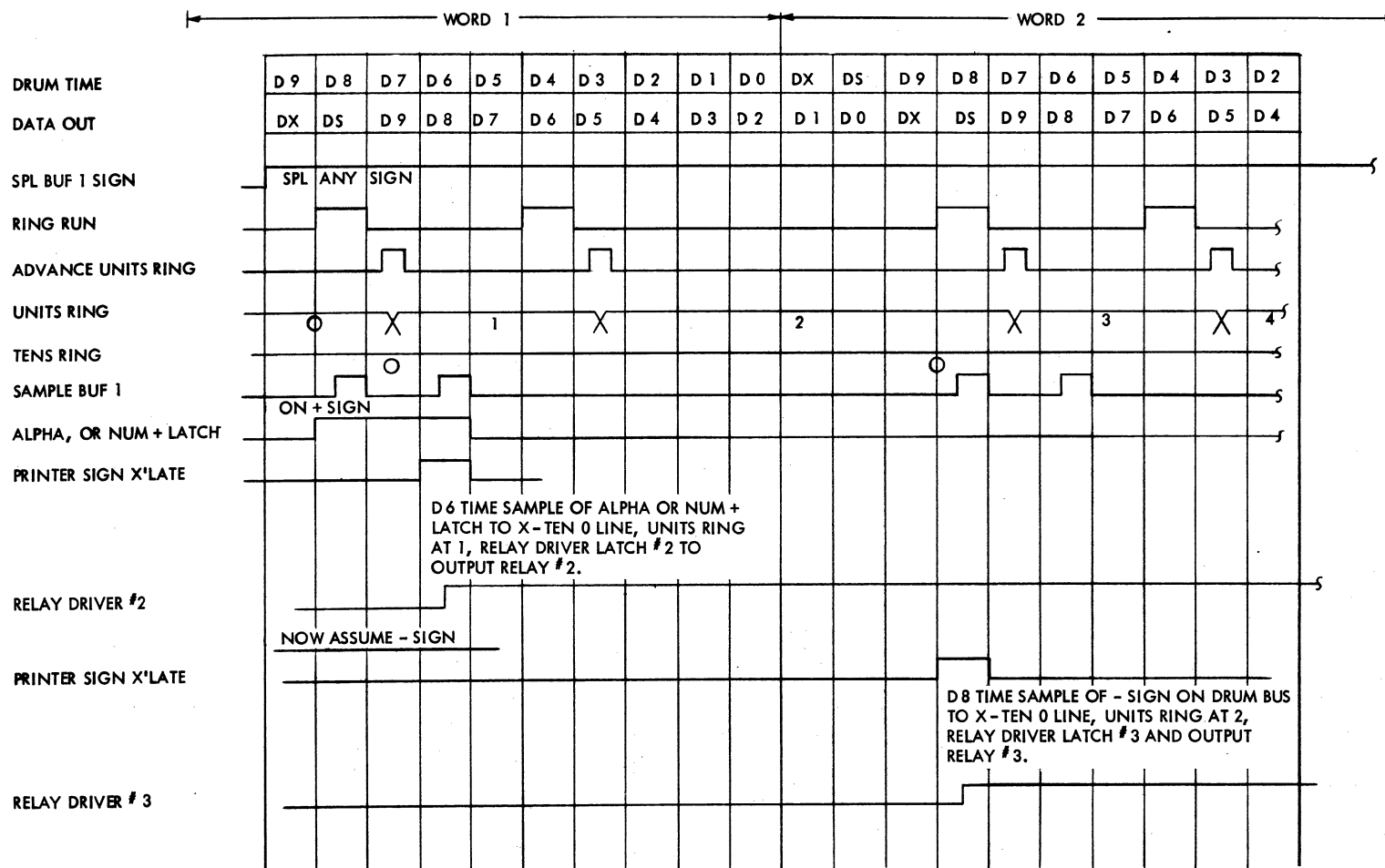


FIGURE 4.1-3 SEQUENCE FOR PRINTER SIGN RO